ESE 570 Chip Input and Output (I/O) Circuits

OVERVIEW

1. INPUT PADS – ESD PROTECTION

2. TTL-TO-CMOS LOGIC LEVEL SHIFTING

3. DIFFERENTIAL SIGNALING

4. OUTPUT PADS – L di/dt NOISE

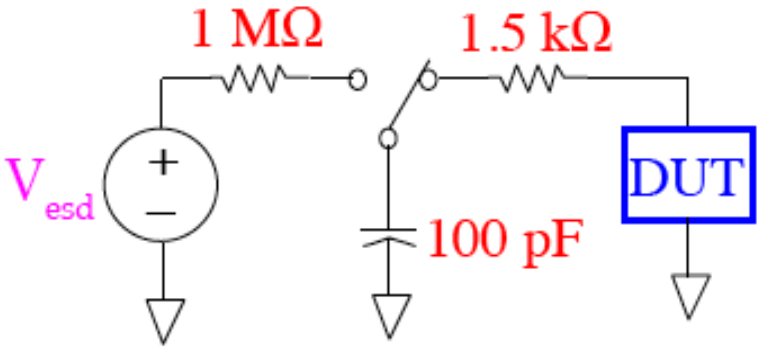
5. BIDIRECTIONAL I/O PADS

6. ON-CHIP CLOCK GENERATION AND DISTRIBUTION

7. LATCH-UP PROTECTION IN OUTPUT PADS

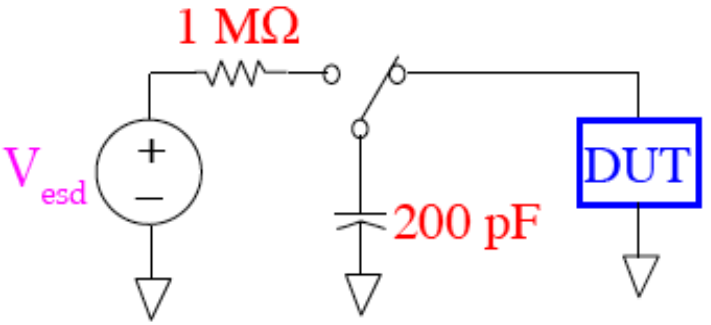
ESD PROTECTION

Human Body Model (HBM)



Simulates the touch from a charged human's finger.

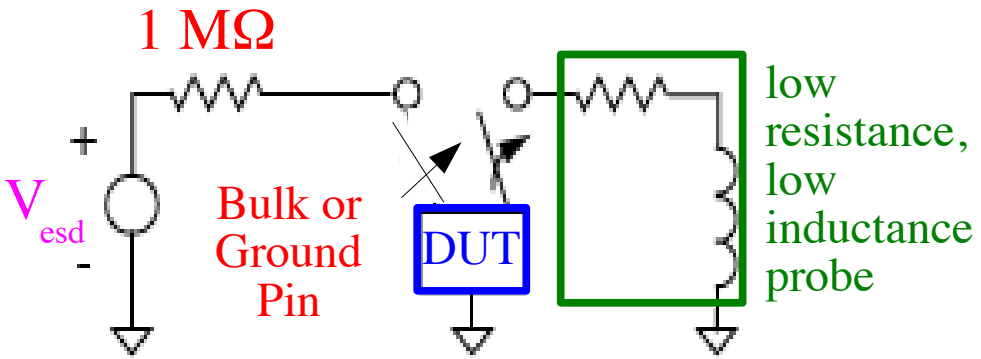
Machine Model (MM)



Since in MM body resistance is absent, contact with machines can be higher stress.

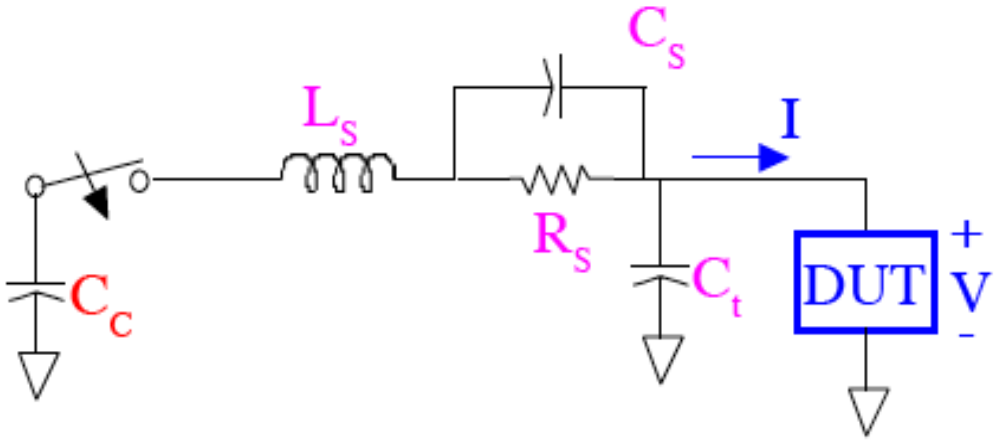
Charged-Device Model (CDM)

Electrostatic charge builds up on a chip due to improper grounding and then discharges when a low-resistance path becomes available.

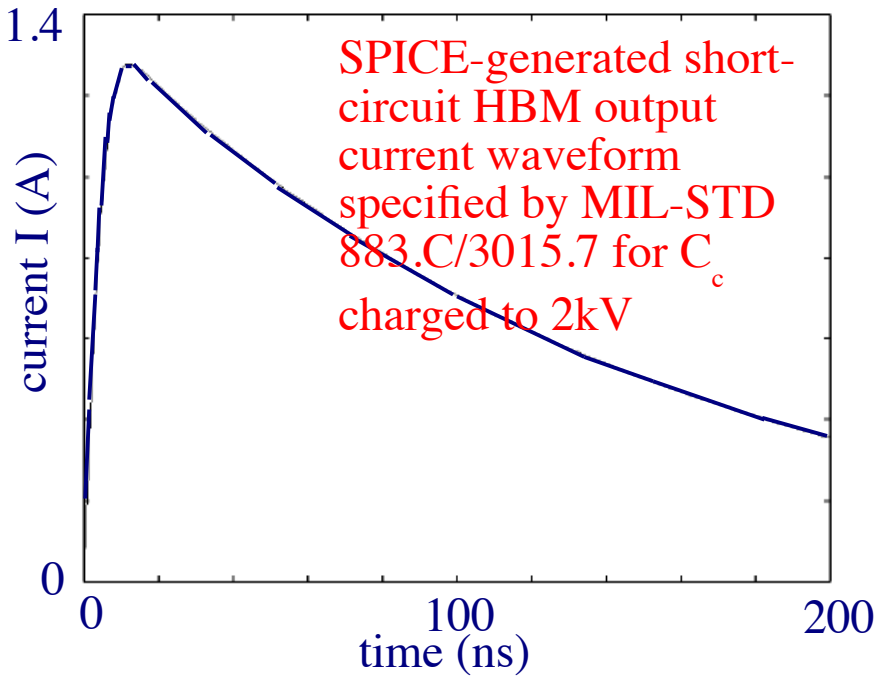


Simulates ESD phenomena of packaged ICs during manufacturing and assembly.

ATE HBM ESD and MM ESD TEST SETUP

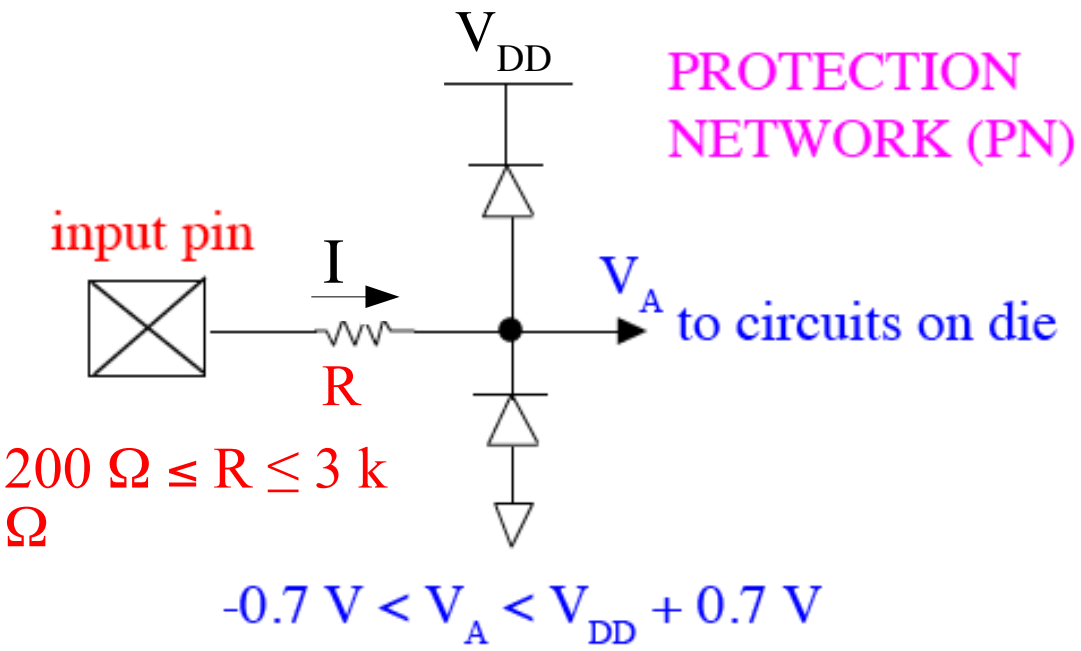


Component	HBM	MM
C_c (pF)	100	200
R_s (Ω)	1500	25
L_s (μH)	5	2.5
C_s (pF)	1	0
C_t (pF)	10	10



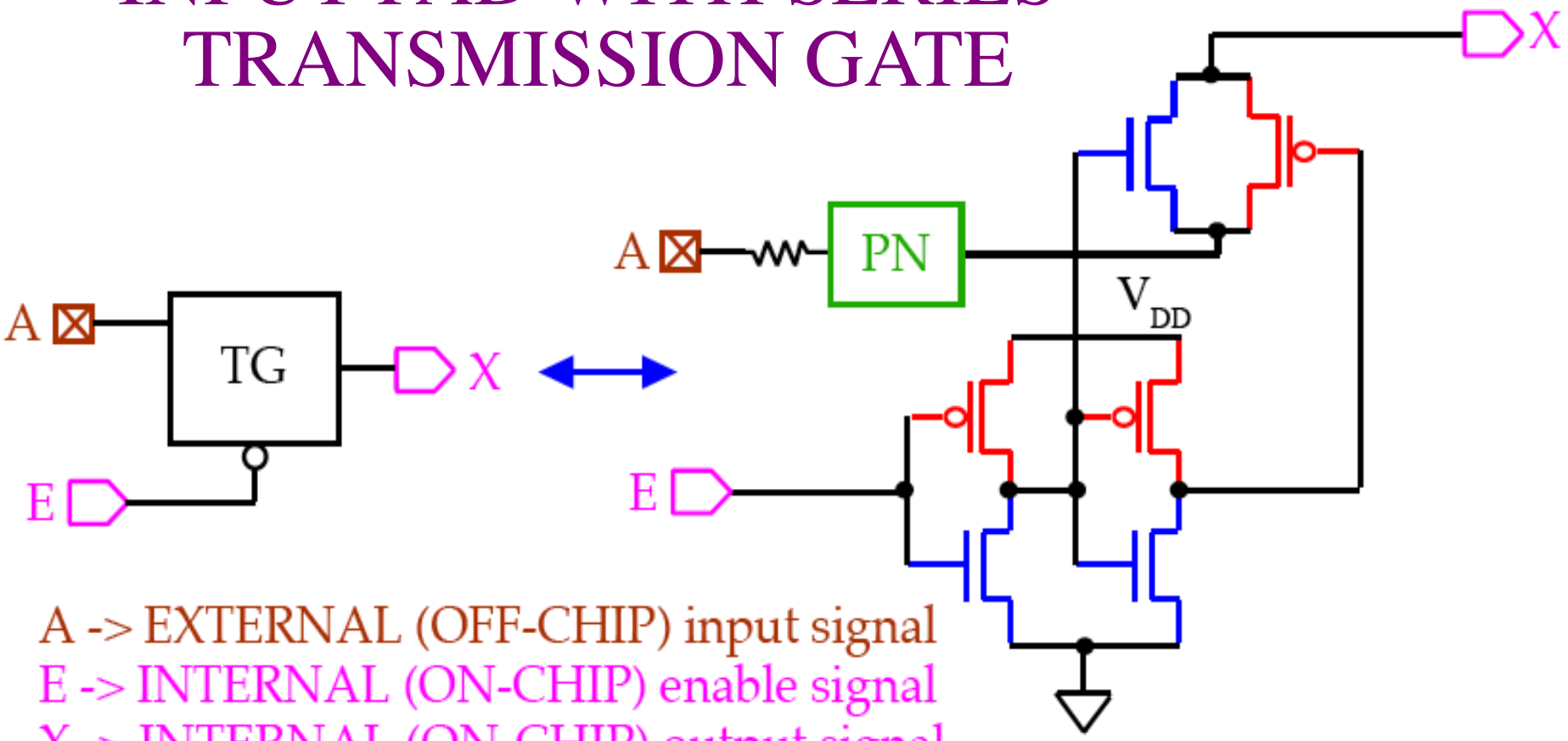
After exposure to the ESD waveform, a failed IC exhibits latch-up or fails one or more data sheet specifications.

TYPICAL ESD PROTECTED INPUT PAD



Effective protection networks can withstand up to 8 kV HBM ESD stress or $8A \geq I \geq 2.6$ A.

INPUT PAD WITH SERIES TRANSMISSION GATE

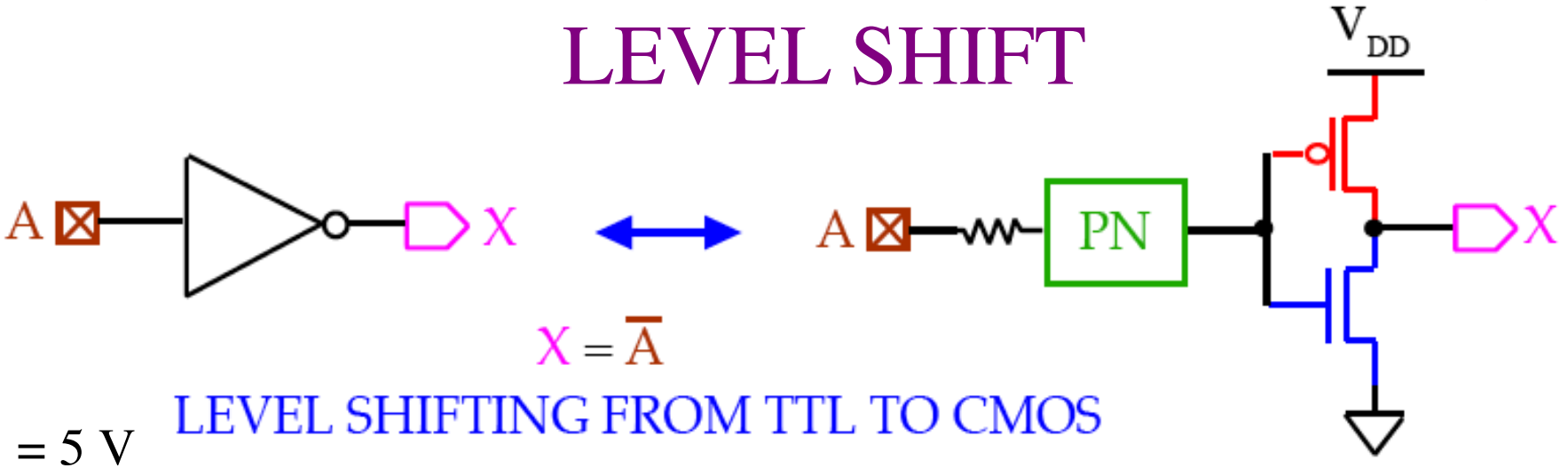


A -> EXTERNAL (OFF-CHIP) input signal
E -> INTERNAL (ON-CHIP) enable signal
X -> INTERNAL (ON-CHIP) output signal

X = A, when E = 0
X = HIGH-IMPEDANCE STATE when E = 1

NOTE: ANY UNUSED INPUT TERMINALS SHOULD BE TIED TO V_{DD} OR GND USING WEAK PULL-UP OR PULL-DOWN TRANSISTORS RATHER THAN FLOAT

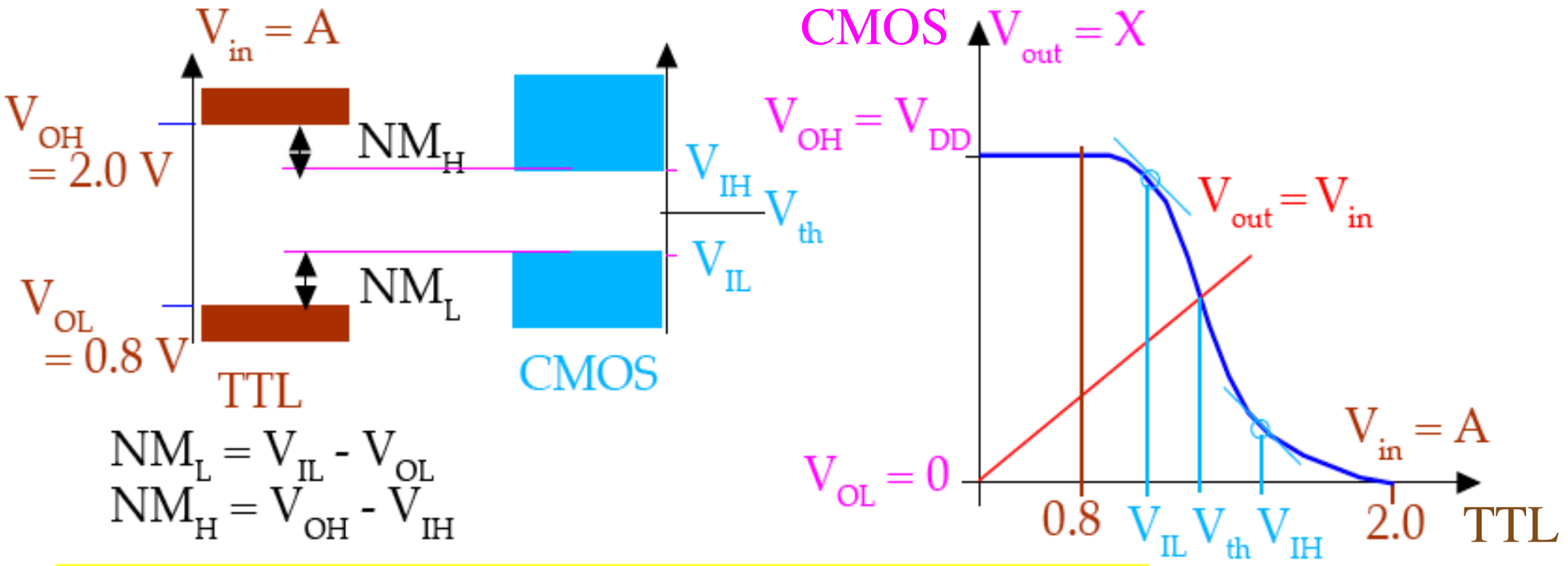
INVERTING INPUT PAD WITH TTL-TO-CMOS LEVEL SHIFT



$X = \overline{A}$

LEVEL SHIFTING FROM TTL TO CMOS

$V_{DD} = 5$ V



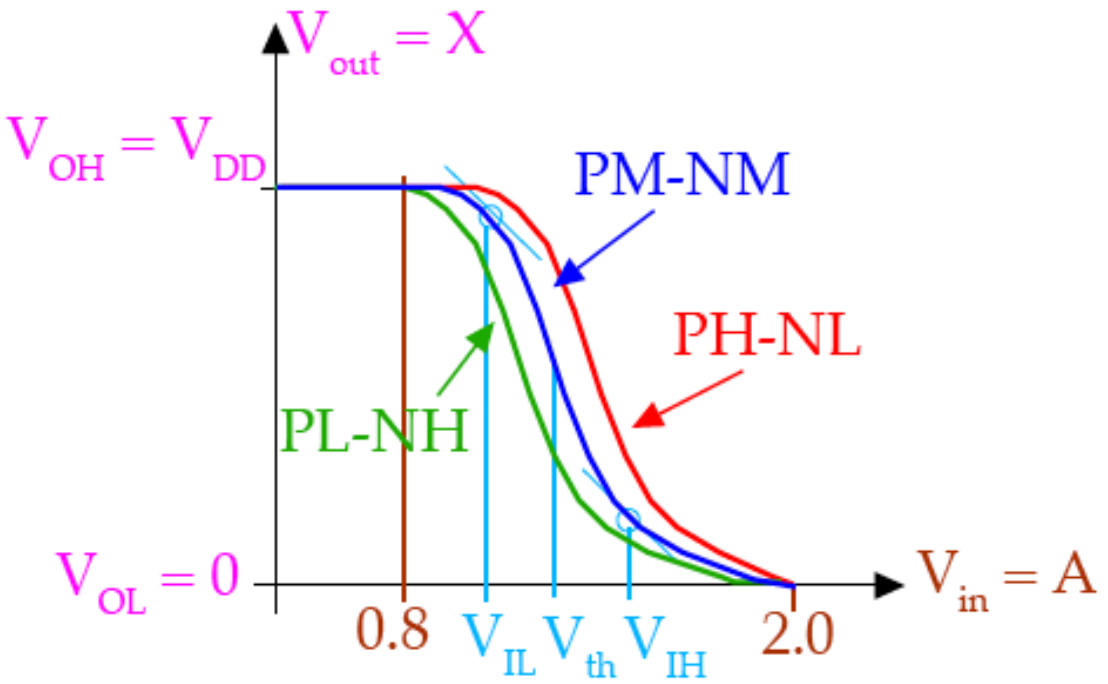
$NM_L = V_{IL} - V_{OL}$

$NM_H = V_{OH} - V_{IH}$

DESIGN FOR $V_{th} = 0.8\text{ V} + (2.0\text{ V} - 0.8\text{ V})/2 = 1.4\text{ V}$

VARIATIONS IN LEVEL-SHIFT VTC DUE TO PROCESS VARIATIONS

8x



PM-NM => nominal processing
PH-NL => strong pMOS, weak nMOS process corner
PL-NH => weak pMOS, strong nMOS process corner

IN ADDITION:
Strong (fast) nMOS, pMOS -> low V_{Tn0}, low $|V_{T0p}|$; high k_n, high k_p
Weak (slow) nMOS, pMOS -> high V_{Tn0}, high $|V_{T0p}|$; low k_n, low k_p

WORST CASE SIMULATION METHOD

Models are first partitioned into their main types, that is NMOS, PMOS, R, and C. All possible combinations of these types are then run. However, in practice, in order to reduce the number of simulation runs R and C are grouped together.

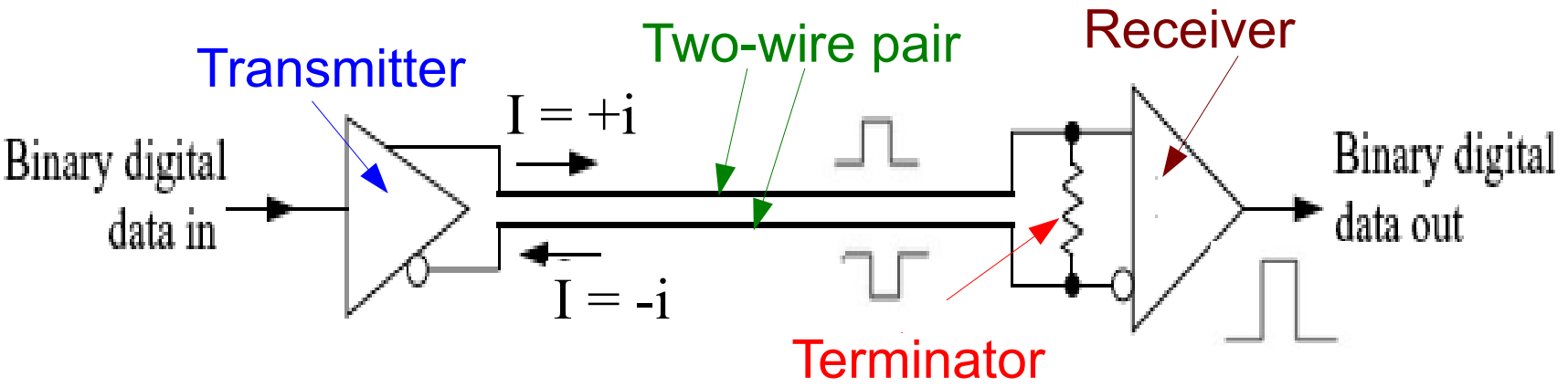
For example, if a design contained NMOS and PMOS, the following sets would be run:

1. weak nmos, weak pmos, temp.
2. weak nmos, nominal pmos, temp.
3. weak nmos, strong pmos, temp.
4. nominal nmos, weak pmos, nominal temp.
5. nominal nmos, nominal pmos, nominal temp.
6. nominal nmos, strong pmos, nominal temp.
7. strong nmos, weak pmos, high temp.
8. strong nmos, nominal pmos, high temp.
9. strong nmos, strong pmos, high temp.

A total of 9 runs.

If R and C are included, the number of runs would increase to 27.

Differential Signaling System



DIFFERENTIAL SIGNALING (LOGIC LEVELS) FOR GBPS SYSTEMS

LVPECL (low-voltage positive referenced emitter coupled logic)
LVDS (low-voltage differential signals)
HSTL (highspeed transceiver logic)
CML (current-mode logic)

Table 1. Typical LVPECL, LVDS, HSTL, and CML Outputs

Output	LVPECL	LVDS	HSTL	CML
V_{OH} (Min)	2.275 V	1.400 V	VDDQ[1] - 0.4	V_{CC}[2]
V_{OL} (Max)	1.68 V	1.000 V	0.400 V	V_{CC} - 0.4 V

Table 2. Typical LVPECL, LVDS, CML, and HSTL Input Levels

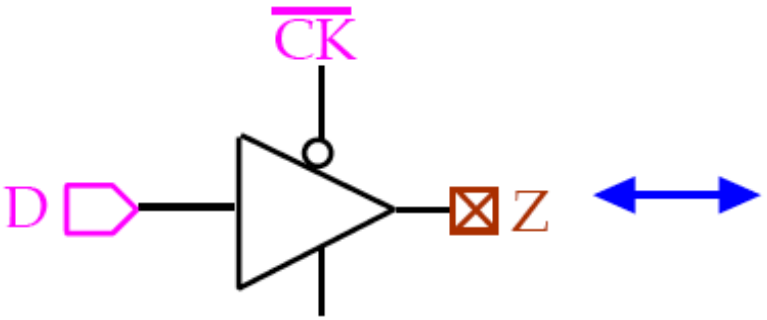
Input	LVPECL	LVDS	HSTL	CML
V_{IH} (Min)	2.135 V	1.220 V	VRef + 0.2	V_{CC}
VRef or VCM	2	1.2	0.75	V_{CC} - 0.2 V
V_{IL} (Max)	1.825 V	1.100 V	VRef -0.2	V_{CC} - 0.4 V
V_{ID} (Min)	310 mV	200 mV	400 mV	400 mV

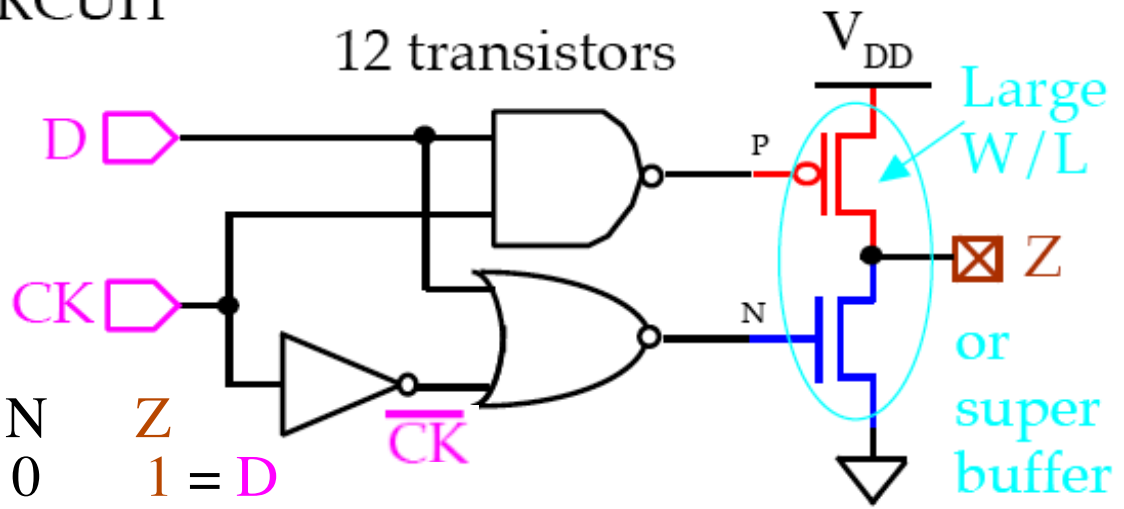
1 $VDDQ = 1.5V \pm 10\%$

2 $V_{CC} = 3.3V \pm 10\%$

OUTPUT PADS

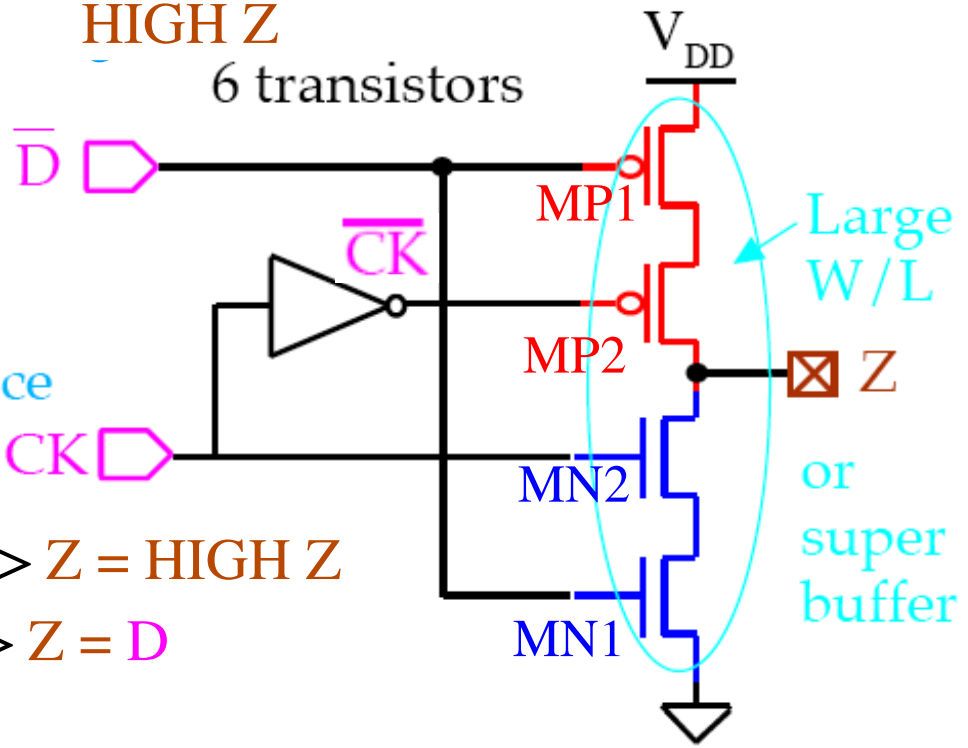
TRISTABLE OUTPUT CIRCUIT





CK	D	P	N	Z
1	1	0	0	1 = D
1	0	1	1	0 = D
0	x	1	0	HIGH Z

Z = D for CK = 1
Z = HIGH IMP for CK = 0



LARGE W/L
-> Sufficent current sink, source
-> Reduce delay times

CK = 0 => MN2 & MP2 OFF => Z = HIGH Z

CK = 1 => MN2 & MP2 ON => Z = D

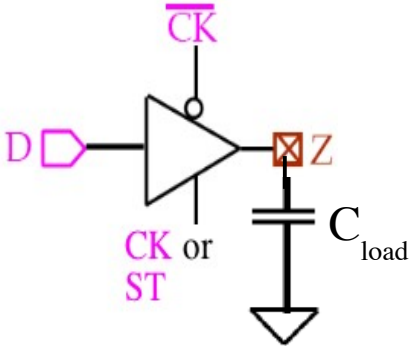
OUTPUT PADS – L di/dt NOISE

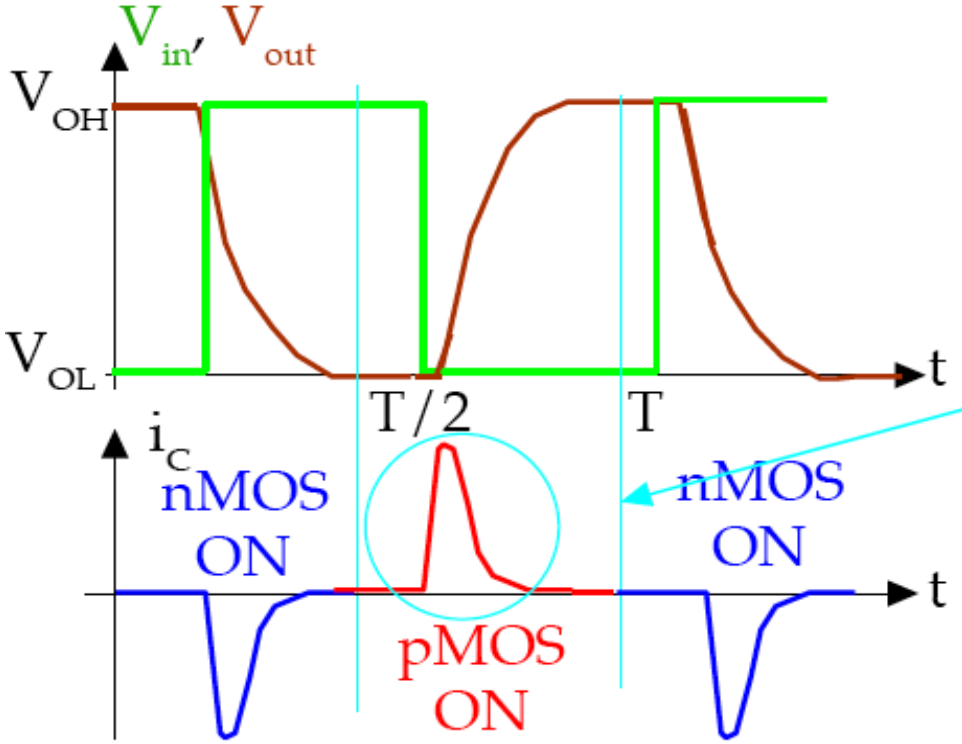
LARGE W/L

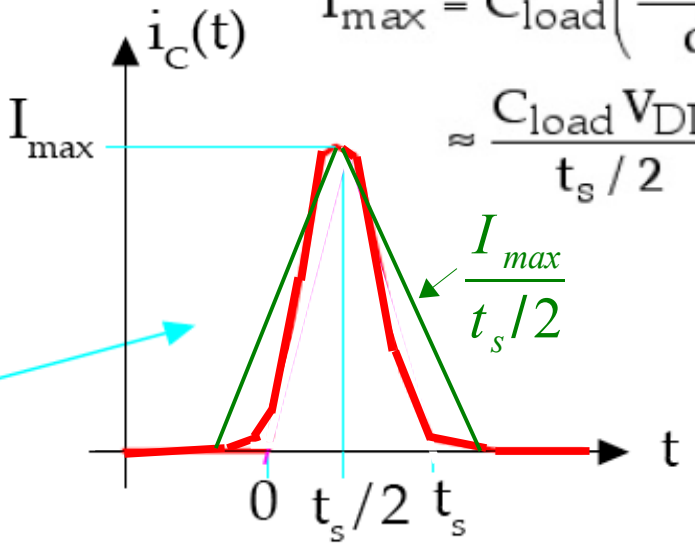
-> Sufficient current sink, source => LARGE di/dt

-> Reduce delay times

L (di/dt) VOLTAGE DROP ACROSS BONDING WIRE CONNECTING PAD TO PACKAGE PIN







$$I_{max} = C_{load}\left(\frac{dV_{out}}{dt}\right)_{max} \approx \frac{C_{load}\,V_{DD}}{t_s/2}$$

assume C_{load} charged to V_{DD}

$$\left[\frac{di}{dt}\right]_{max} \geq \frac{I_{max}}{t_s/2} = \frac{2\,I_{max}}{t_s} \geq \frac{4\,C_{load}\,V_{DD}}{(t_s)^2}$$

≈ 0.1 to 10 A/ns

OUTPUT PADS – L di/dt NOISE

$$\left[\frac{di}{dt}\right]_{max} \geq \frac{4\,C_{load}\,V_{DD}}{(t_s)^2}$$

LET C_{load} = 1 pF, L = 1 nH, V_{DD} = 3.5 V and t_s = 1 ns

$$\left[\frac{di}{dt}\right]_{max} \geq \frac{4\times\left(1\times10^{-12}\,\frac{C}{V}\right)\times 3.5\,V}{\left(1\times10^{-9}\,s\right)^2} = \frac{14\times10^{-12}\,A}{1\times10^{-9}\,ns} = 14\,\frac{mA}{ns}$$

$$L\left[\frac{di}{dt}\right]_{max} \geq 14mV$$

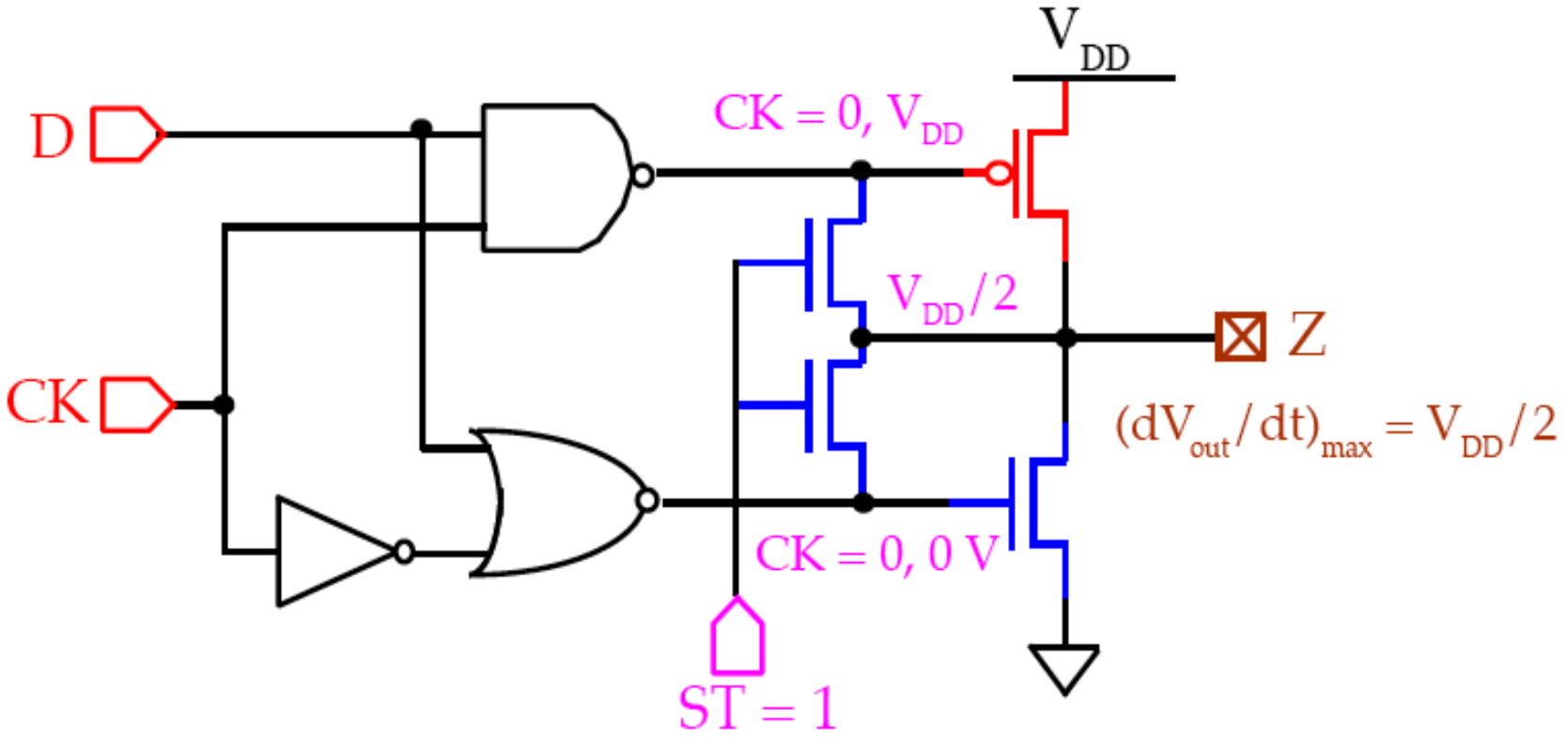
HIGH-END MICROPROCESSOR CHIPS WITH 32 BITS OR 64 BIT DATA BUS LINES - ALL OTPUT DRIVERS SWITCHING AT THE SAME TIME!

For 32 bits switching simulataneously:

$$32\times L\left[\frac{di}{dt}\right]_{max} \approx 0.45\,V$$ PROBLEM!

REDUCE NOISE => lower V_{DD} or increase t_s -> limits speed

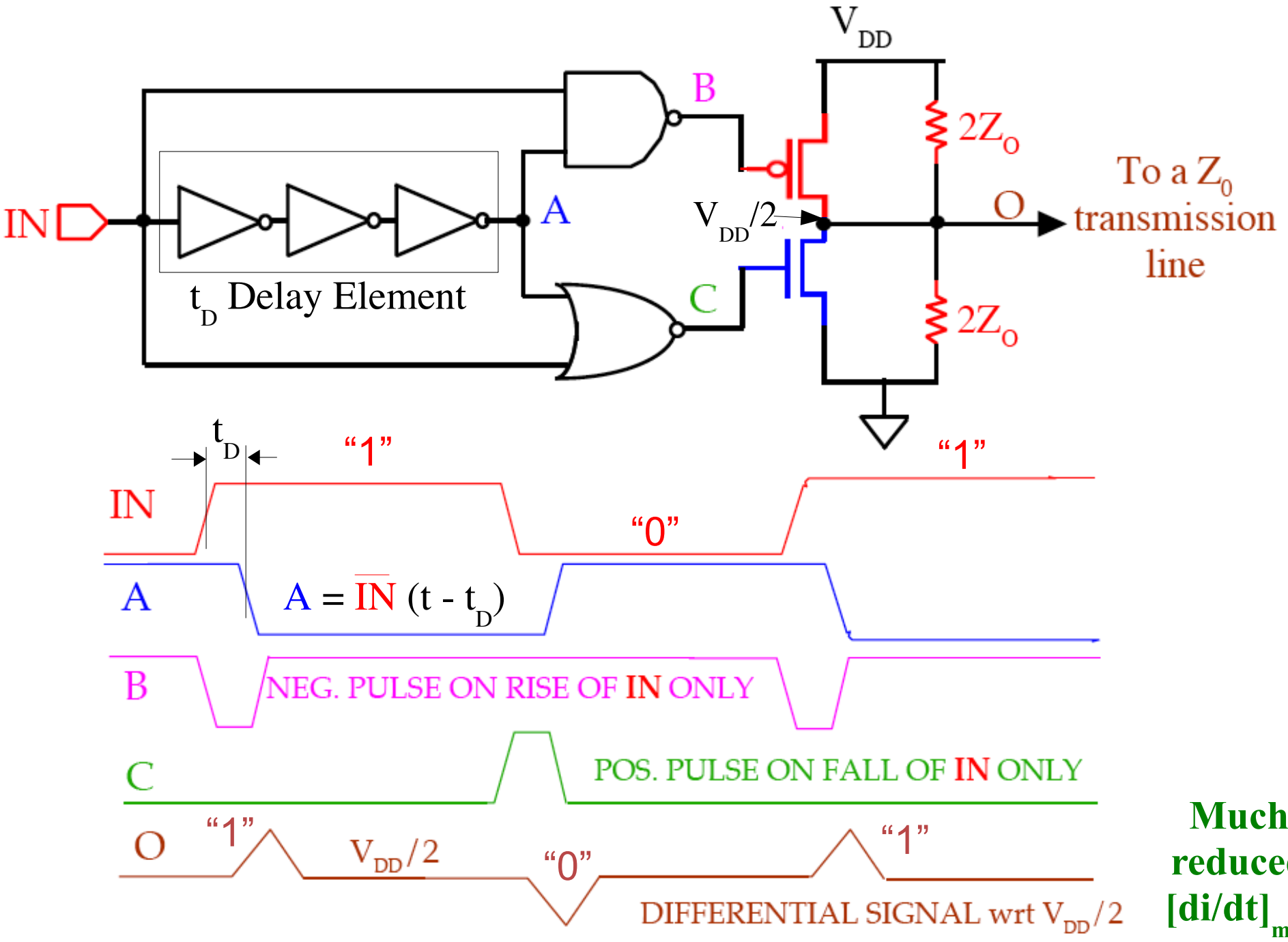
OUTPUT PADS – REDUCE L di/dt NOISE



PRECHARGES INVERTER OUTPUT "Z" TO $V_{DD}/2$ WHEN ST = 1 AND CK = 0 (JUST PRIOR TO CK -> 1)

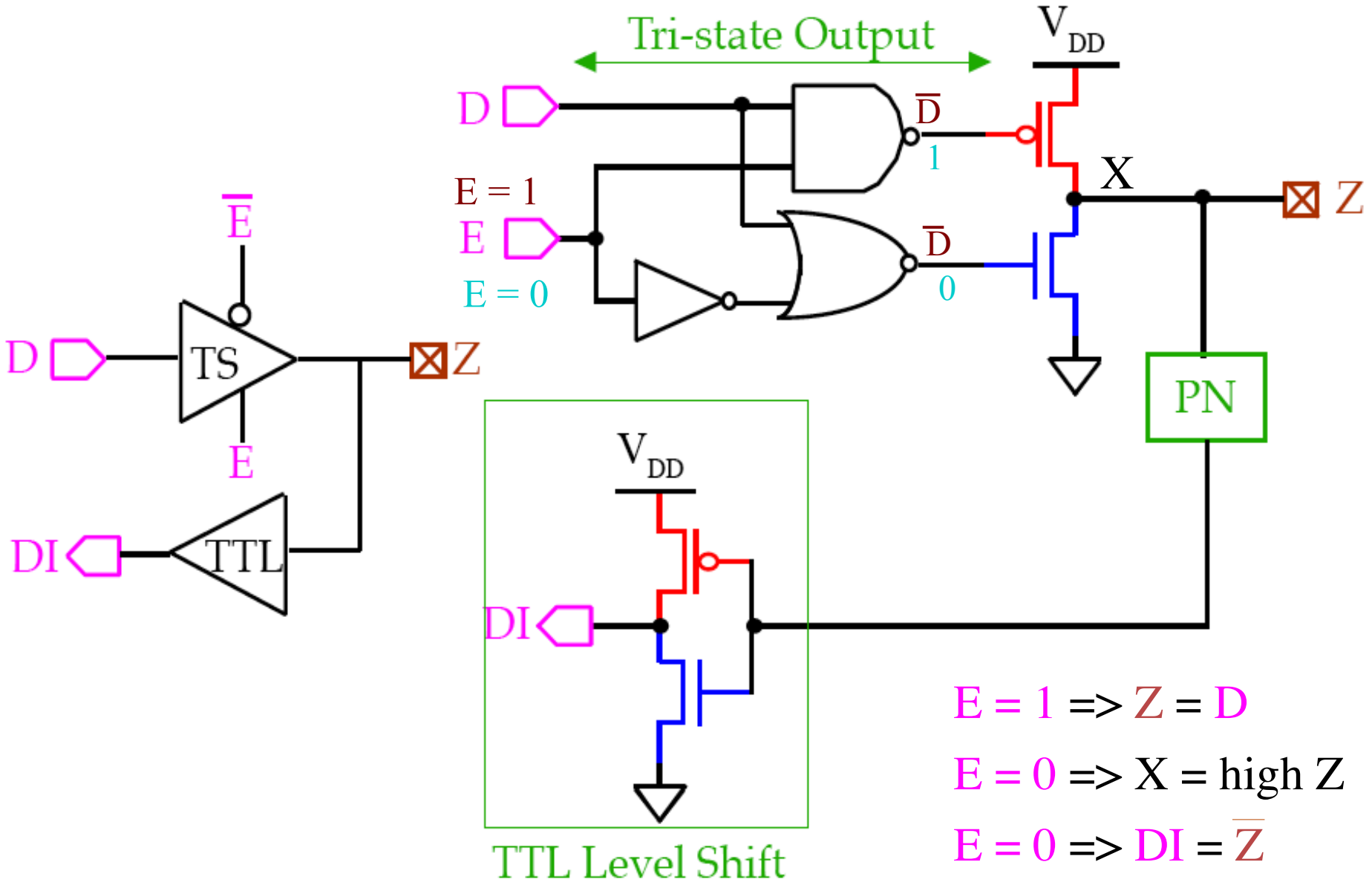
ALSO, STAGGER SWITCHING TIMES OF 32 OUTPUT DRIVERS BY USING BULT-IN DELAYS IN THE CLOCK DISTRIBUTION NET.

DIFFERENTIAL DRIVER OUTPUT PAD

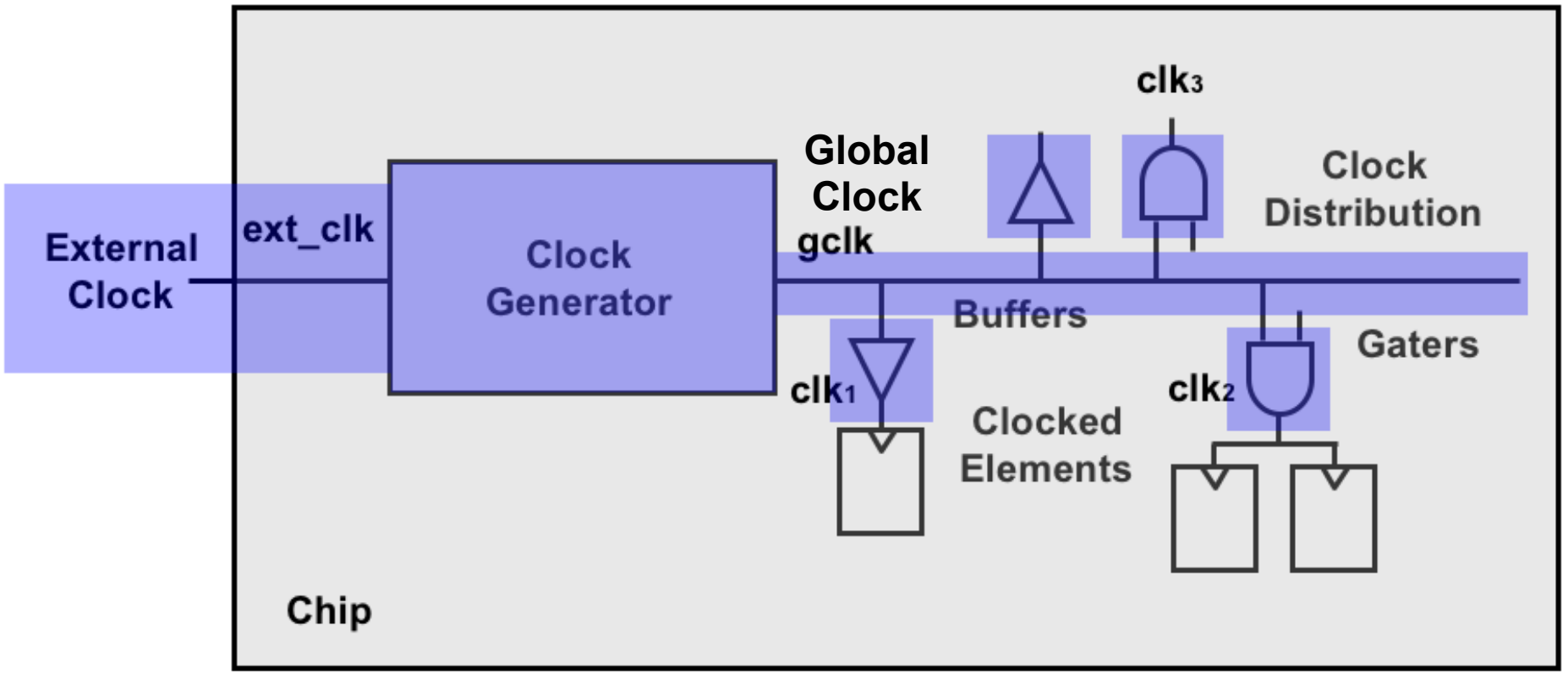


Much reduced $[di/dt]_{max}$

BIDIRECTIONAL I/O PAD WITH TTL INPUT CAPABILITY



Clock System Architecture

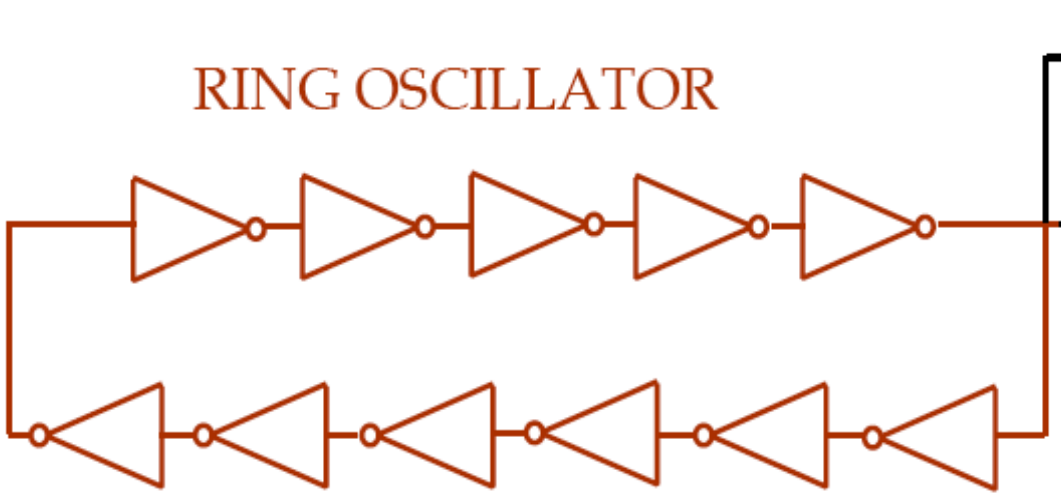


- Chip receives external clock through I/O pad or an internal clock is included in the Clock Generator.
- Clock generator adjusts the global clock to the external clock.
- Global clock is distributed across the chip.
- Local drivers and "clock gaters" drive the physical clocks to clocked elements.

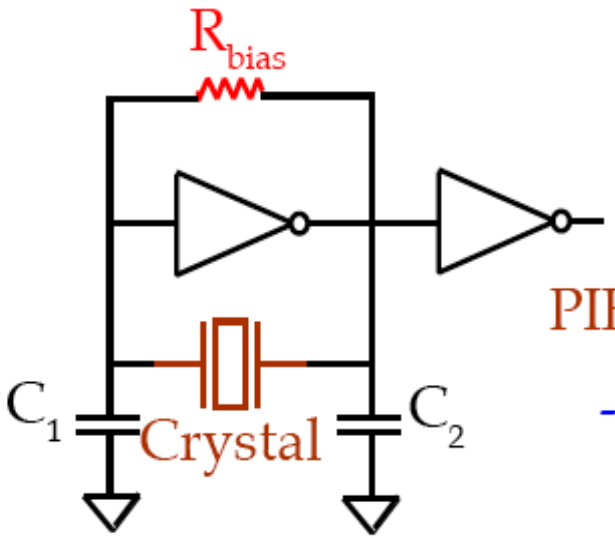
ON-CHIP CLOCK GENERATION AND DISTRIBUTION

SIMPLE ON-CHIP CLOCK CIRCUIT

RING OSCILLATOR



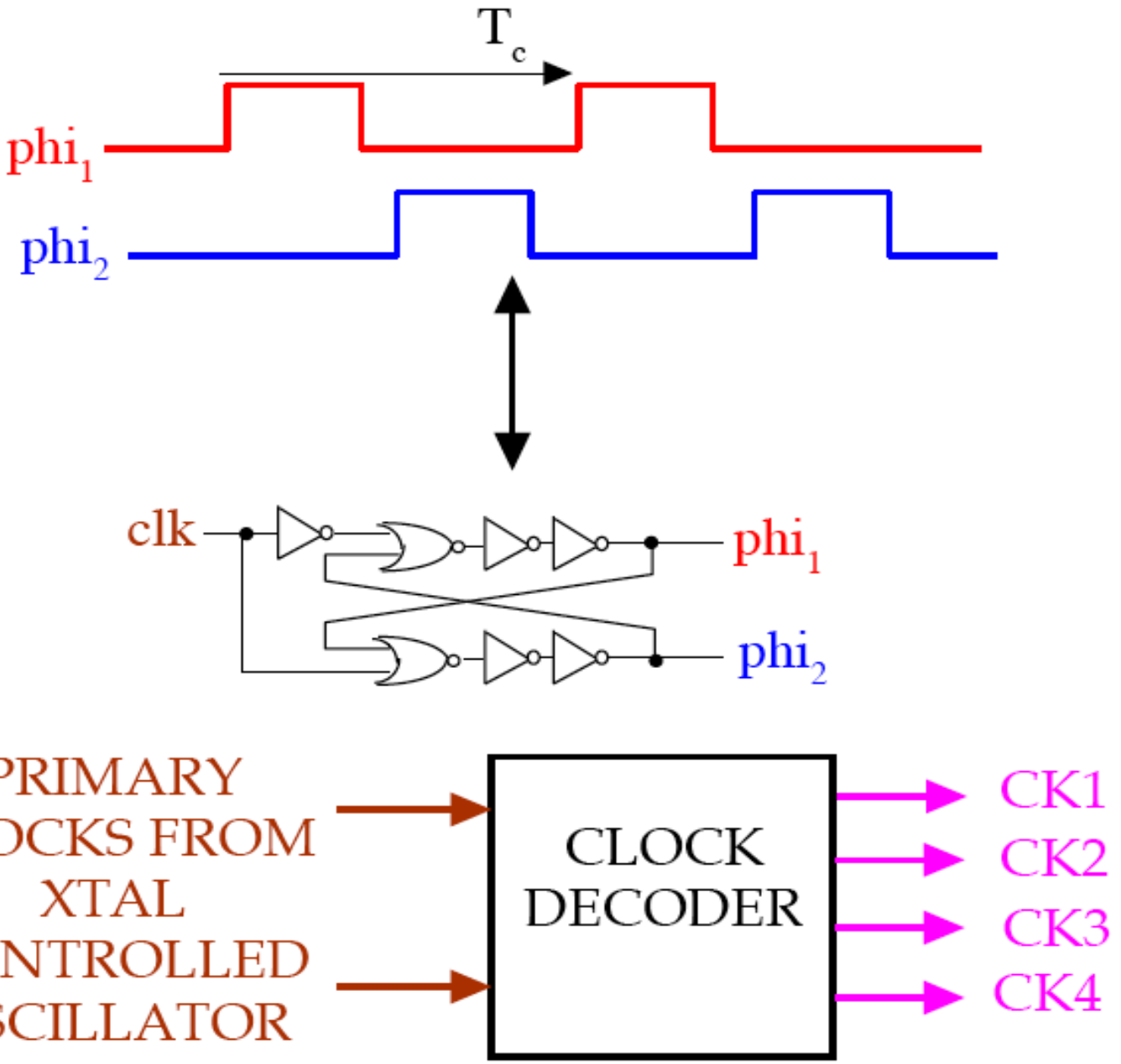
CK FREQUENCY
-> PROCESS DEPENDENT
-> UNSTABLE FREQUENCY



PIERCE CRYSTAL OSCILLATOR CIRCUIT

-> GOOD FREQUENCY STABILITY

TWO-PHASE CLOCK GENERATION



Clock Skew and Jitter

- **Clock should theoretically arrive simultaneously to all sequential circuits.**
- **Practically it arrives in different times. The differences are called *clock skews*.**
- **Most systems distribute a *global clock* and then use local "*clock gaters*" located near clocked elements.**
- **Skews result from paths mismatches, process variations and ambient conditions, resulting in *physical clocks ≠ global clock*.**

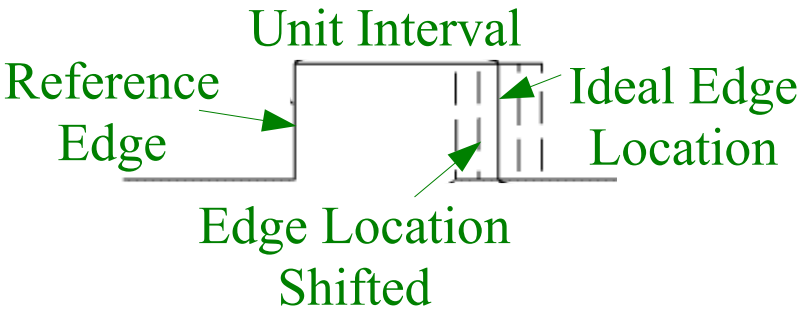
Clock Skew Components

Systematic is the portion of clock skew existing under nominal conditions. It can be minimized by appropriate design.

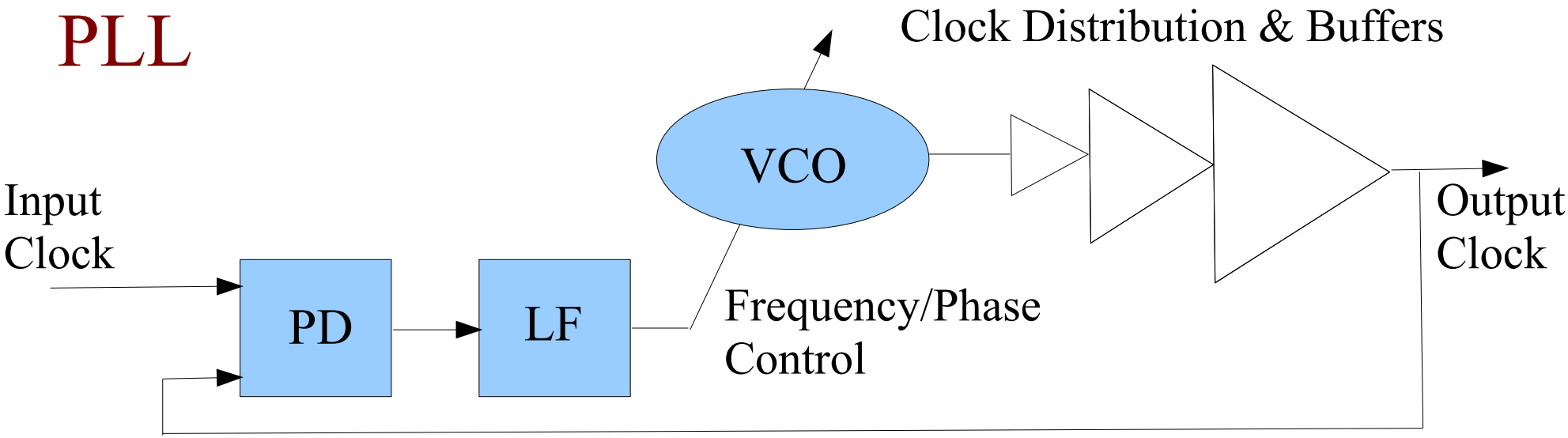
Random is variable portion of clock skew caused by random process variations like devices' channel length, oxide thickness, threshold voltage, wire thickness, width and space. It can be measured on silicon and adjusted by DLL components.

Drift is time-dependent portion of clock skew caused by time-dependent environmental variations, occurring relatively slowly. Compensation of those must takes place periodically.

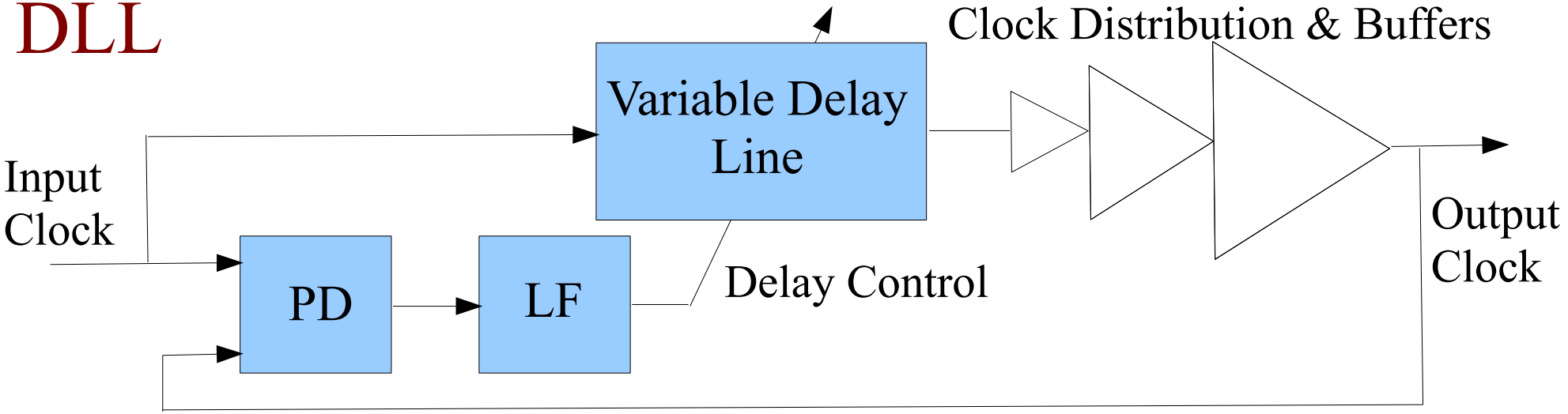
Jitter is rapid clock edge changes (deterministic and random components), occurring by power noise and clock generator jitter. It cannot be compensated.



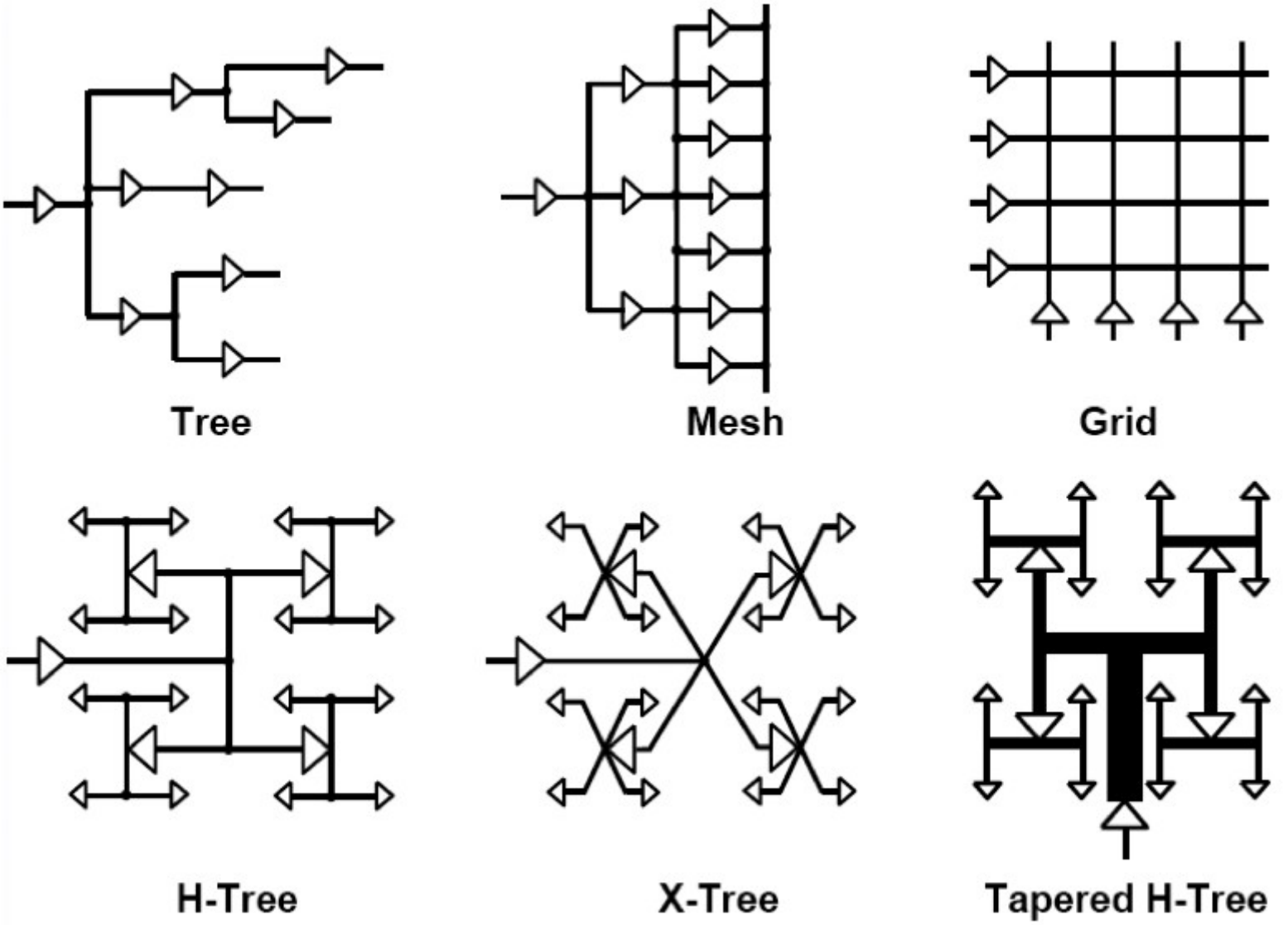
PLL


Clock Distribution & Buffers
VCO
Input
Clock
PD
LF
Frequency/Phase
Control
Output
Clock

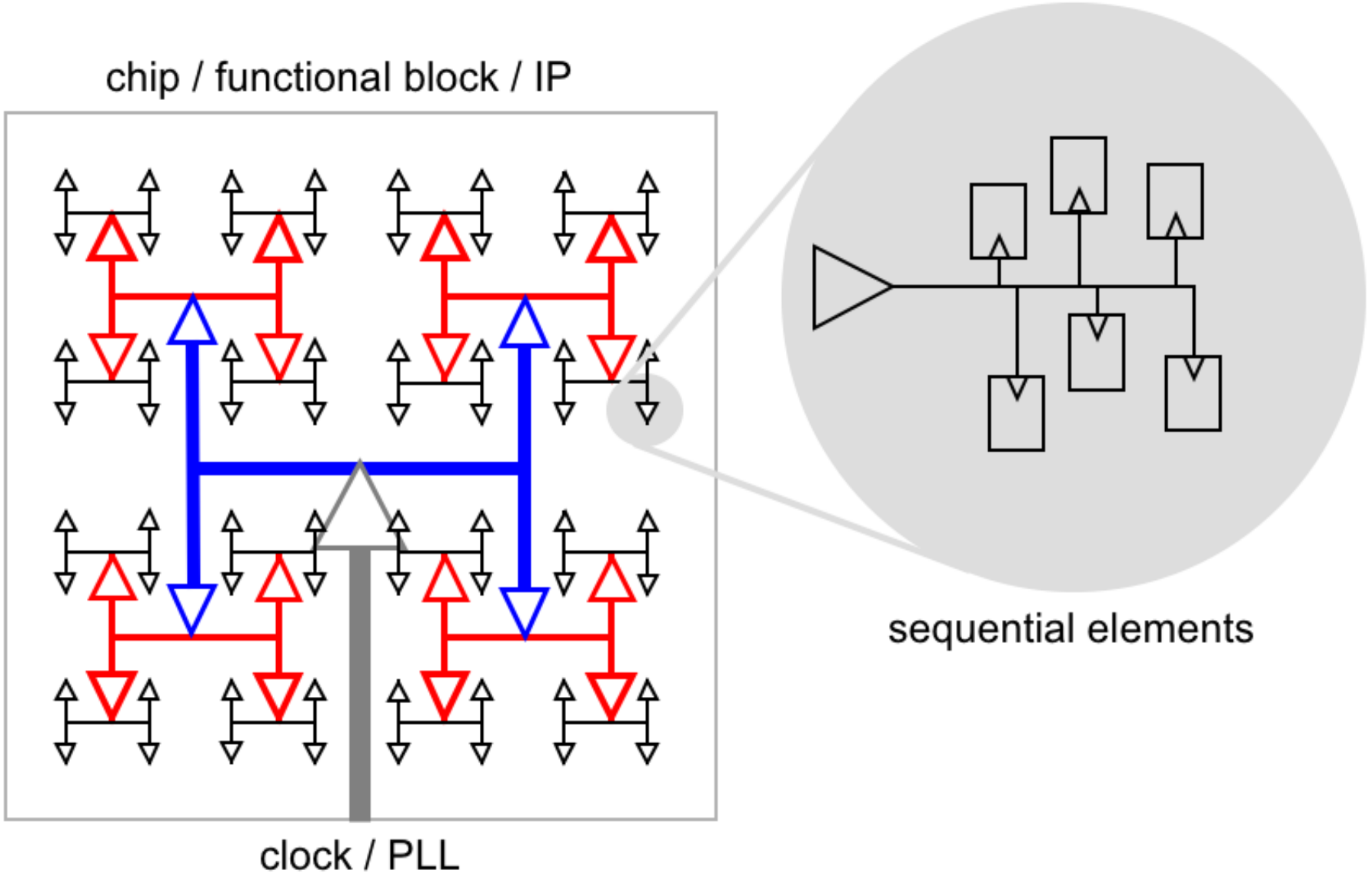
DLL


Clock Distribution & Buffers
Variable Delay
Line
Input
Clock
PD
LF
Delay Control
Output
Clock

Some Representative Clock Distribution Networks



H-TREE CLOCK DISTRIBUTION NET FOR UNIFORM CLOCK DISTRIBUTION

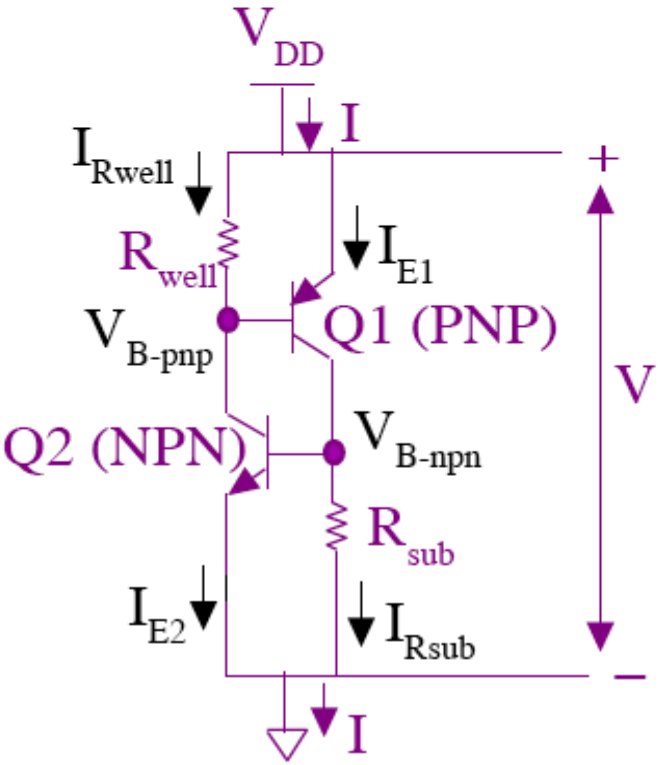


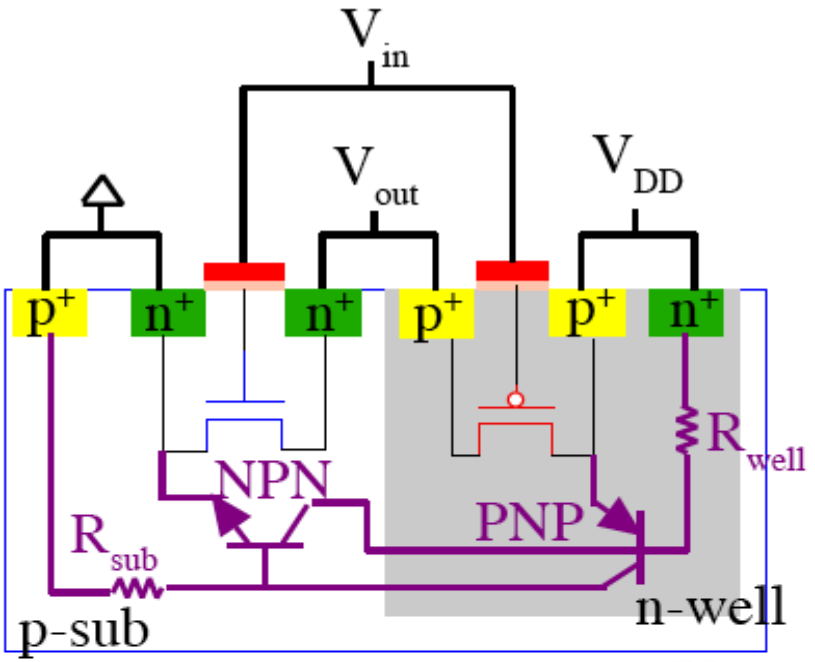
CAD Techniques automate the generation of hierarchical clock distribution networks.

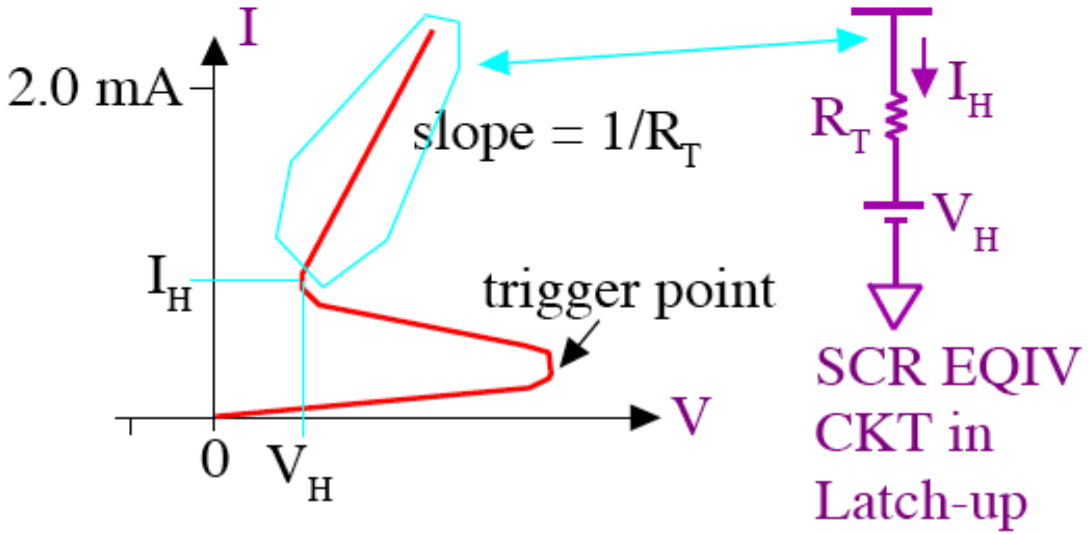
LATCH-UP IN CMOS CIRCUITS

latch-up susceptability proportional to

$$\frac{1}{NSUB} x \left(\frac{1}{nMOS - pMOS\ spacing} \right)^2$$





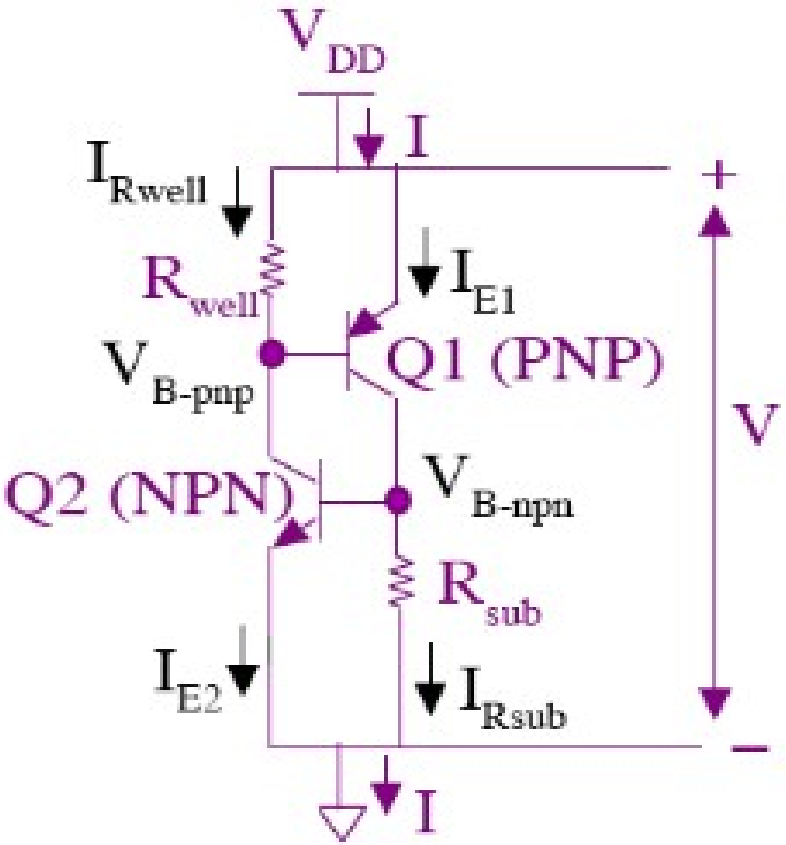


LATCH-UP – POSITIVE FEEDBACK

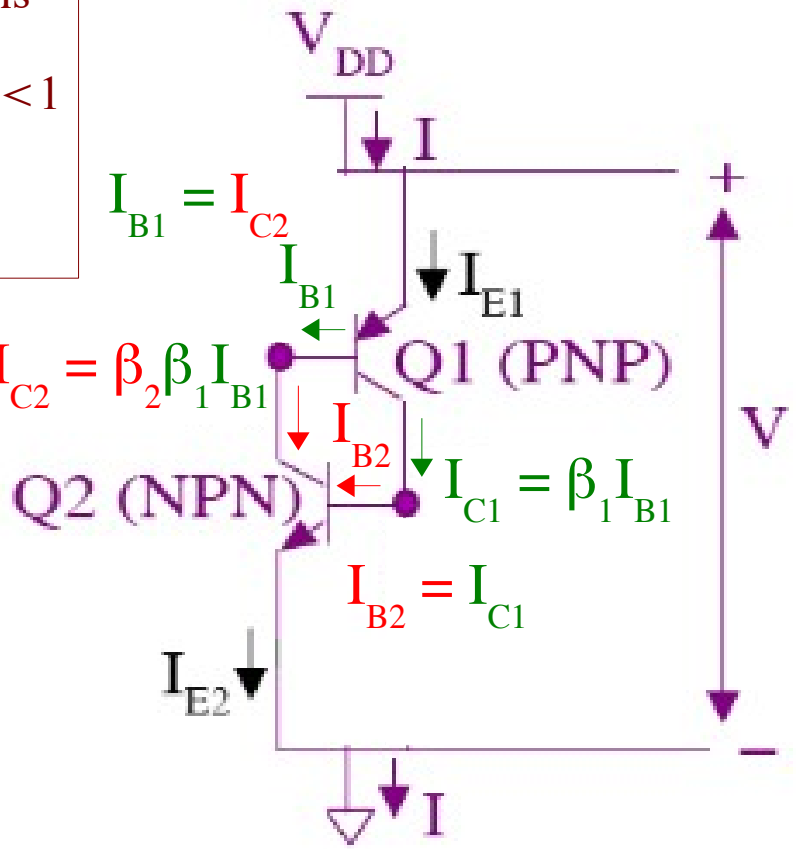
Bipolar Current Gains

$$\beta = \frac{I_C}{I_B} > 1 \quad 0 < \alpha = \frac{I_C}{I_E} < 1$$

$$\beta = \frac{\alpha}{1-\alpha}$$



$$R_{well} = R_{sub} = \infty$$



Latch-up Analysis with $R_{well} = R_{sub} = \infty$

time = t1 > 0:

$I_{B1} = x \Rightarrow I_{C1} = \beta_1 x$

time = t2 > t1

$I_{B2} = I_{C1} = \beta_1 x \Rightarrow I_{C2} = \beta_2 \beta_1 x$

positive feedback! if $\beta_2 \beta_1 \geq 1$

Prevent latch-up by reducing positive feedback

$$\beta_1 \beta_1 = \frac{\alpha_1}{1-\alpha_1} \frac{\alpha_2}{1-\alpha_2} \leq 1 \Rightarrow \alpha_1 + \alpha_2 \leq 1$$

$$\beta_1 \beta_2 \leq 1$$

LATCH-UP PREVENTION

Latch-up prevention with parasitic resistances R_{well} and R_{sub}

$$\alpha_1 + \alpha_2 \leq 1 + \frac{\frac{R_T}{R_{well}}\alpha_1 + \frac{R_T}{R_{sub}}\alpha_2}{\frac{V_{DD}}{V_{BE}} - 2}$$

make large

make small

Latch-up occurs if NOT satisfied

TO PREVENT LATCH-UP: Insure Latchup Condition is Violated!

Reduce α_1, α_2 ; Reduce R_{sub}, R_{well} ; Decrease V_{DD}

A. Use a latchup resistant process.

Latchup Prevention LAYOUT Guidelines:

B. Use p^+ guard rings connected to GND around nMOS transistors and n^+quard rings connected to V_{DD} around the pMOS transistors to reduce R_{well} and R_{sub} and to weaken BJTs.

C. Place sub, well contacts close to the nMOS, pMOS source connections to supply rails (i.e. GND for nMOS, V_{DD} for pMOS) to reduce R_{well} and R_{sub}.

CONSERVATIVE RULE: One sub contact per source connection to a supply, or GND.

LESS CONSERVATIVE: One sub contact per 5-10 transistors.

D. Layout nMOS, pMOS transistors close to GND, VDD rails, respectively and maintain space between nMOS, pMOS transistors.

OUTPUT BUFFER CELL LAYOUT WITH LATCH-UP PREVENTION