CMOS

Digital Integrated Circuits

Analysis and Design

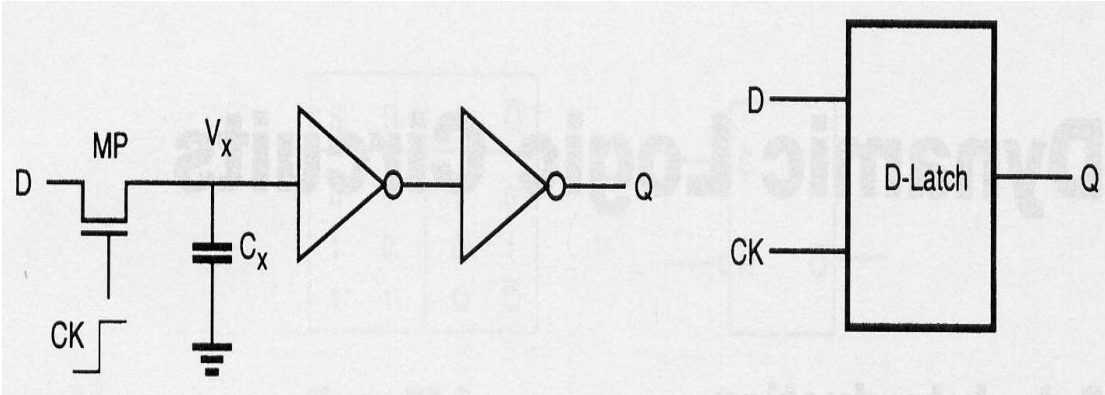
Chapter 9

Dynamic Logic Circuits

Introduction

- Static logic circuit
  - Output corresponding to the input voltage after a certain time delay
  - Preserving its output level as long as the power supply is provided
  - Large area, time delay
- Dynamic logic circuit
  - The operation of all dynamic logic gates depends on temporary (transient) storage of charge in parasitic node capacitances
  - Need periodic clock signals $\Rightarrow$charge refreshing
  - Smaller silicon area
  - Consume less power

Example 9.1



- CK=1, MP on
  - C_x charging, or discharging ⇒ Q=D
- CK=0 MP off
  - C_x isolated from D
  - $Q=V_x$ (depend on the charge store in C_x)
- 2nd inverter remove
  - Transistor counts ↓
  - Q=-D
- Assuming VOL=0V, VIL=2.1V, VIH=2.9V, VOH=5.0V, VTn=0.8V
  - CK=1, MP on
    - Vin=VOH=5V, Vx=5-0.8=4.2V, higher than VIH so VQ=VDD
  - CK=0, M off
    - Vx=4.2V, if charge leakage ⇒ Vx<2.9V, can't be interpreted as a logic "1"

Basic principles of pass transistor circuits

- The fundamental building block of nMOS dynamic logic circuits
  - An nMOS pass transistor driving the gate of another nMOS transistor
- MP
  - Driving by the periodic clock sign
  - Acts as access switch
  - If CK=1
    - Logic "1" transfer
    - Logic "0" transfer
  - If CK=0
    - Cease to conduct and the charge store In the parasitic capacitance

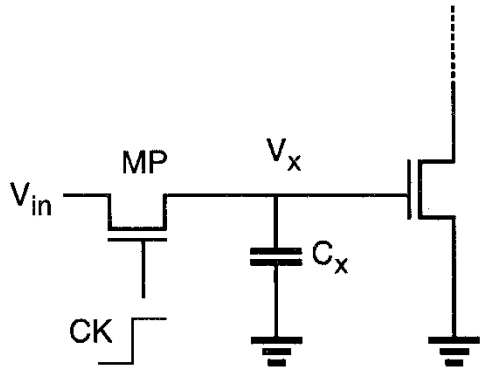


Figure 9.1 The basic building block for nMOS dynamic logic, which consists of an nMOS pass transistor driving the gate of another nMOS transistor.

Logic "1' transfer

Intially $V_x(t=0) = 0V$, $V_{in} = V_{OH} = V_{DD}$, $CK: 0 \rightarrow 1$

MP on in saturation region starts to charge up the C_x

$$C_x \frac{dV_x}{dt} = \frac{k_n}{2}\left(V_{DD} - V_x - V_{T,n}\right)^2$$

$$\int_0^t dt = \frac{2C_x}{k_n}\int_0^{Vx} \frac{dV_x}{\left(V_{DD} - V_x - V_{T,n}\right)^2} = \frac{2C_x}{k_n}\left(\frac{1}{\left(V_{DD} - V_x - V_{T,n}\right)}\right)\Bigg|_0^{V_x}$$

$$t = \frac{2C_x}{k_n}\left[\left(\frac{1}{\left(V_{DD} - V_x - V_{T,n}\right)}\right) - \left(\frac{1}{\left(V_{DD} - V_{T,n}\right)}\right)\right]$$

$$V_x(t) = \left(V_{DD} - V_{T,n}\right)\frac{\left(\frac{k_n\left(V_{DD} - V_{T,n}\right)}{2C_x}\right)t}{1 + \left(\frac{k_n\left(V_{DD} - V_{T,n}\right)}{2C_x}\right)t}$$

$$V_{max} = V_x\Big|_{t\rightarrow\infty} = V_{DD} - V_{T,n} = V_{DD} - V_{T0,n} - \gamma\left(\sqrt{\left|2\phi_F\right| + V_{max}} - \sqrt{\left|2\phi_F\right|}\right)$$

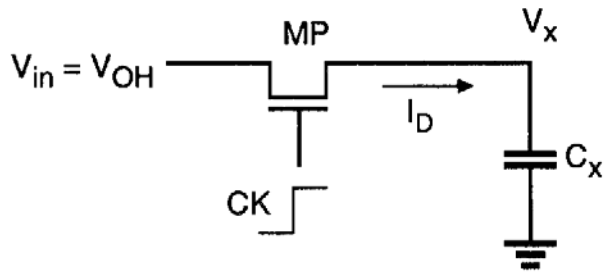


Figure 9.2 Equivalent circuit for the logic "1" transfer event.

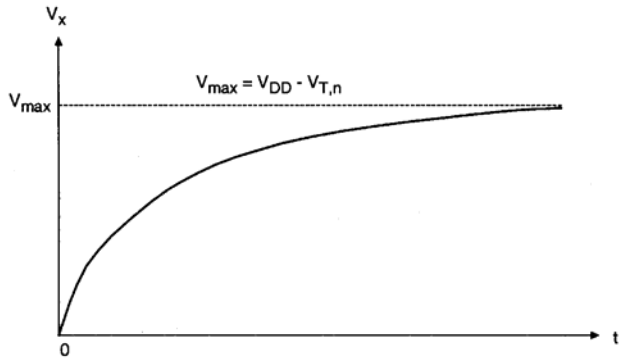


Figure 9.3 Variation of V_x as a function of time during logic "1" transfer.

The node V_x has an upper limit of $V_{max}=(V_{DD}-V_{T,n})$

Logic "1' transfer

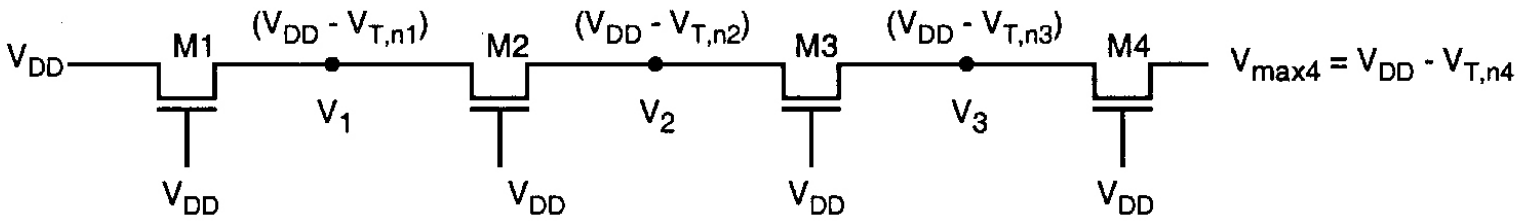


Figure 9.4 Node voltages in a pass-transistor chain during the logic "1" transfer

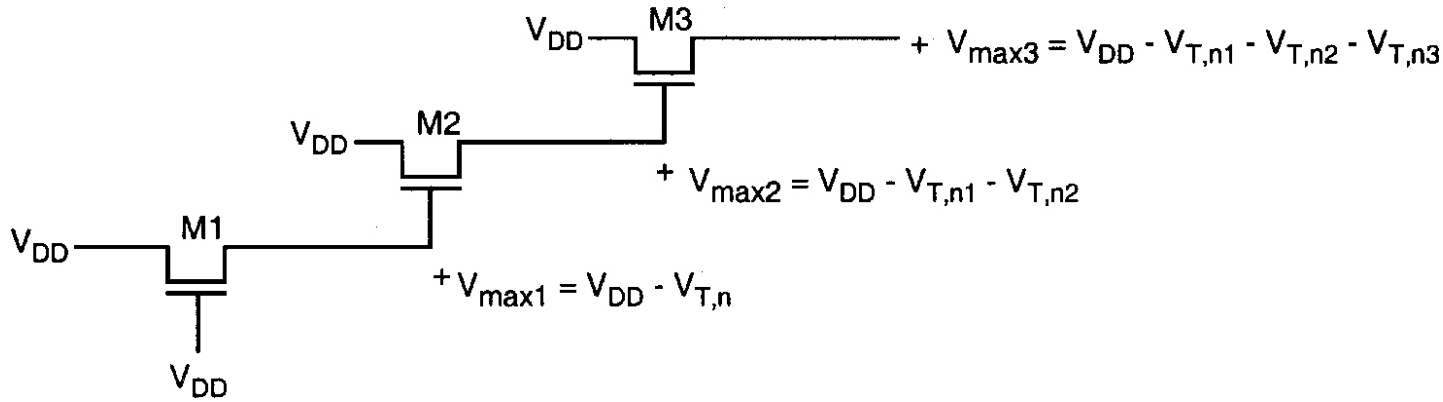


Figure 9.5 Node voltages during the logic "1" transfer, when each pass transistor is driving another pass transistor.

$$V_{T,n1} = V_{T0,n} - \gamma\left(\sqrt{|2\phi_F| + V_{\max 1}} - \sqrt{|2\phi_F|}\right)$$

$$V_{T,n2} = V_{T0,n} - \gamma\left(\sqrt{|2\phi_F| + V_{\max 2}} - \sqrt{|2\phi_F|}\right)$$

....

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Logic "0" transfer

The pass transistor operates in the linear region throughout this cycle, since $V_{DS}<V_{GS}-V_{T,n}$

$$-C_x\frac{dV_x}{dt}=\frac{k_n}{2}\left(2(V_{DD}-V_{T,n})V_x-V_x^2\right)$$

$$dt=-\frac{2C_x}{k_n}\cdot\frac{dV_x}{2(V_{DD}-V_{T,n})V_x-V_x^2}$$

$$\int_0^t dt=-\frac{2C_x}{k_n}\int_{VDD-VT,n}^{Vx}\left(\frac{1}{2(V_{DD}-V_{T,n})\left(2(V_{DD}-V_{T,n})-V_x\right)}+\frac{1}{2(V_{DD}-V_{T,n})V_x}\right)dV_x$$

$$t=\frac{C_x}{k_n(V_{DD}-V_{T,n})}\left[\ln\left(\frac{2(V_{DD}-V_{T,n})-V_x}{Vx}\right)\right]\Bigg|_{V_{DD}-V_{T,n}}^{V_x}$$

$$t=\frac{C_x}{k_n(V_{DD}-V_{T,n})}\ln\left(\frac{2(V_{DD}-V_{T,n})-V_x}{V_x}\right)$$

$$t_{90\%}=\frac{C_x}{k_n(V_{DD}-V_{T,n})}\ln\left(\frac{(2-0.9)(V_{DD}-V_{T,n})}{0.9(V_{DD}-V_{T,n})}\right)=\frac{C_x}{k_n(V_{DD}-V_{T,n})}\ln\left(\frac{1.1}{0.9}\right)$$

$$t_{10\%}=\frac{C_x}{k_n(V_{DD}-V_{T,n})}\ln\left(\frac{1.9}{0.1}\right)$$

$$\tau_{fall}=t_{10\%}-t_{90\%}=\frac{C_x}{k_n(V_{DD}-V_{T,n})}\left[\ln(19)-\ln(1.22)\right]=2.74\frac{C_x}{k_n(V_{DD}-V_{T,n})}$$

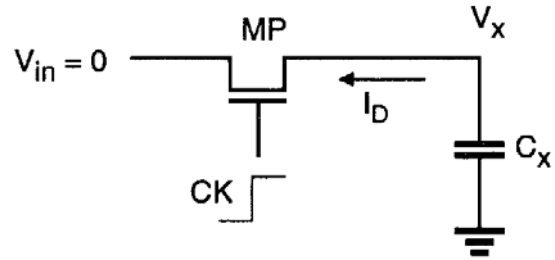


Figure 9.6 Equivalent circuit for the logic "0" transfer event.

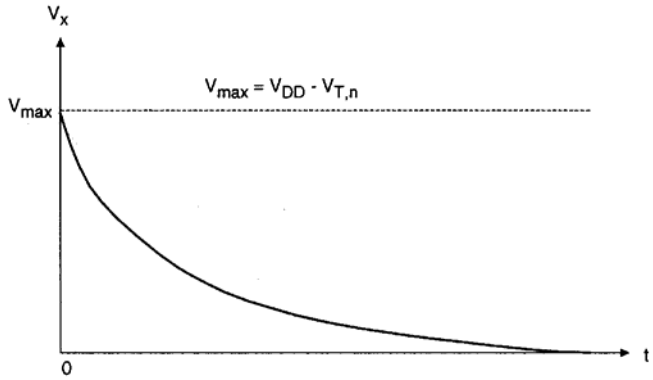


Figure 9.7 Variation of V_x as a function of time during logic "0" transfer.

Charge storage and charge leakage

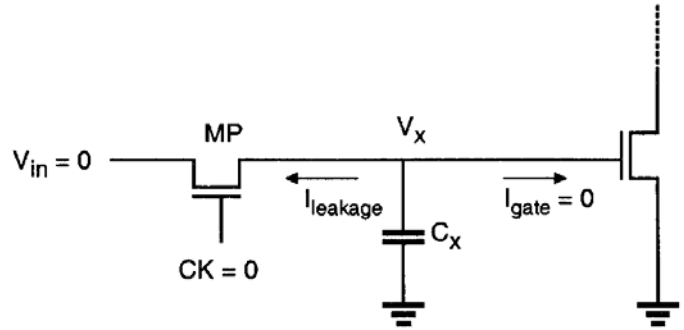


Figure 9.8 Charge leakage from the soft node.

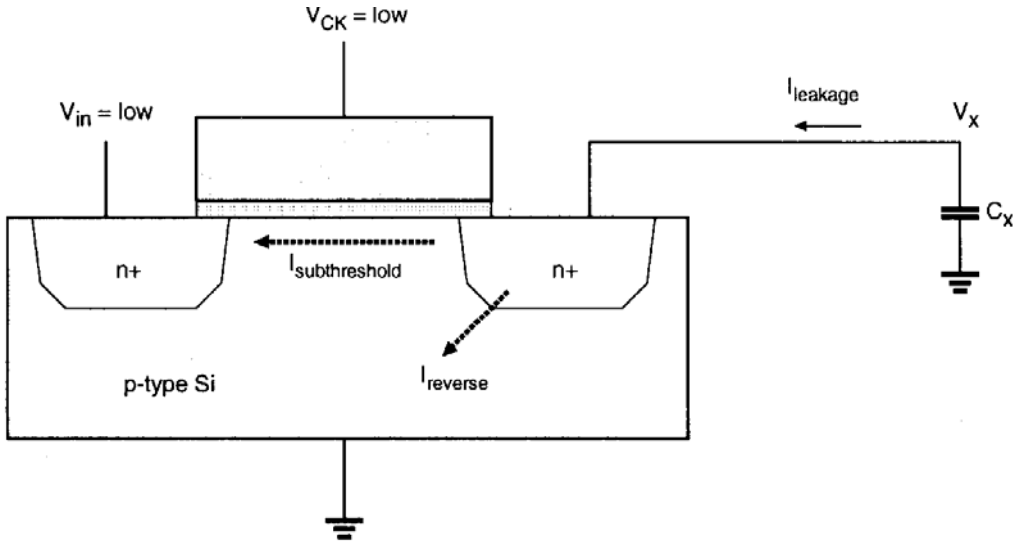


Figure 9.9 Simplified cross-section of the nMOS pass transistor, showing the leakage current components responsible for draining the soft-node capacitance C_x.

$$I_{leakage} = I_{subthreshold(MP)} + I_{reverse(MP)}$$

Equivalent circuit used for analyzing the charge leakage process

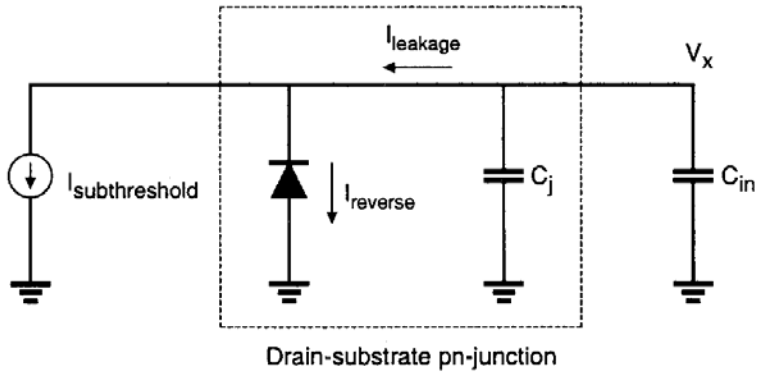


Figure 9.10 Equivalent circuit used for analyzing the charge leakage process.

$$Q = Q_j(V_x) + Q_{in} \quad where\ Q_{in} = C_{in} \cdot V_x$$

$$C_{in} = C_{gb} + C_{poly} + C_{metal}$$

$$I_{leakage} = \frac{dQ}{dt} = \frac{dQ_j(V_x)}{dt} + \frac{dQ_{in}}{dt}$$

$$where\ \frac{dQ_j(V_x)}{dV_x} = C_j(V_x) = \frac{A \cdot C_{j0}}{\sqrt{1 + \frac{V_x}{\phi_0}}} = A \cdot \sqrt{\frac{q\varepsilon_{Si} N_A}{2(\phi_0 + V_x)}}$$

$$\phi_0 = \frac{kT}{q} \ln\left(\frac{N_D \cdot N_A}{n_i^2}\right), C_{j0} = \sqrt{\frac{q\varepsilon_{Si} N_A N_D}{2(N_A + N_D)\phi_0}} \approx \sqrt{\frac{q\varepsilon_{Si} N_A}{2\phi_0}}$$

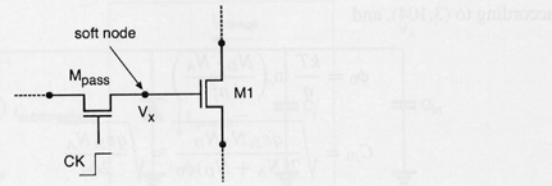
$$C_{x,\min} = C_{gb} + C_{poly} + C_{metal} + C_{db,\min}$$

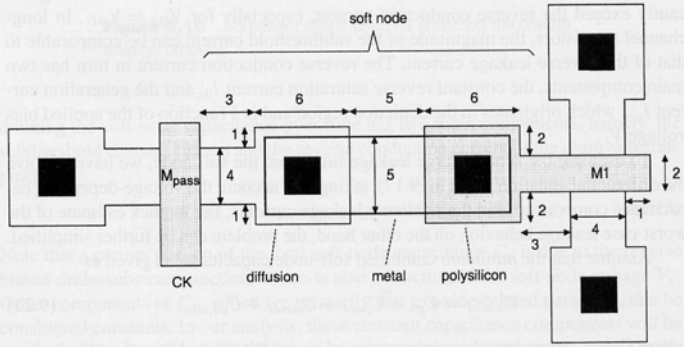
$$t_{hold} = \frac{\Delta Q_{critical,\min}}{I_{leakage,\max}} \text{ where } \Delta Q_{critical,\min} = C_{x,\min}\left(V_{\max} - \frac{V_{DD}}{2}\right)$$

C_{in}: these constant capacitance components
C_x: due to reverse biased drain-substrate junction
$C_{x,min}$: the minimum combined soft-node capacitance
$C_{db.mim}$: the minimum junction capacitance, obtained under the bias condition V_x=V_{max}
t_{hold}: worst-case holding time—the shortest time required for the soft-node voltage to drop from the initial logic high value to the logic threshold voltage due to leakage

Example 2

Consider the soft-node structure shown on the next page, which consists of the drain (or source, depending on current direction) terminal of the pass transistor, connected to the polysilicon gate of an nMOS driver transistor via a metal interconnect.





We will assume that the power supply voltage used in this circuit is $V_{DD} = 5$ V, and that the soft node has initially been charged up to its maximum voltage, V_{max}. In order to estimate the worst-case holding time, the total soft-node capacitance must be calculated first. The simplified mask layout of the structure is shown in the following. All dimensions are given in micrometers. The critical material parameters to be used in this example are listed below.

$$V_{T0} = 0.8 \text{ V}$$
$$\gamma = 0.4 \text{ V}^{1/2}$$
$$|2\phi_F| = 0.6 \text{ V}$$
$$C_{ox} = 0.065 \text{ fF}/\mu\text{m}^2$$
$$C'_{metal} = 0.036 \text{ fF}/\mu\text{m}^2$$
$$C'_{poly} = 0.055 \text{ fF}/\mu\text{m}^2$$
$$C_{j0} = 0.095 \text{ fF}/\mu\text{m}^2$$
$$C_{j0sw} = 0.2 \text{ fF}/\mu\text{m}$$

Example 2 (cont.)

First, we calculate the oxide-related (constant) parasitic capacitance components associated with the soft node.

$$\begin{aligned} C_{gb} &= C_{ox} \cdot W \cdot L_{mask} \\ &= 0.065\ \text{fF}/\mu\text{m}^2 \cdot (4\ \mu\text{m} \times 2\ \mu\text{m}) \\ &= 0.52\ \text{fF} \\ C_{metal} &= 0.036\ \text{fF}/\mu\text{m}^2 \cdot (5\ \mu\text{m} \times 5\ \mu\text{m}) \\ &= 0.90\ \text{fF} \\ C_{poly} &= 0.055\ \text{fF}/\mu\text{m}^2 \cdot (36\ \mu\text{m}^2 + 8\ \mu\text{m}^2) \\ &= 2.42\ \text{fF} \end{aligned}$$

Now, we have to calculate the parasitic junction capacitance associated with the drain-substrate pn-junction of the pass transistor. Using the zero-bias unit capacitance values given here, we obtain

$$\begin{aligned} C_{db,max} &= C_{bottom} + C_{sidewall} \\ &= A_{bottom} \cdot C_{j0} + P_{sidewall} \cdot C_{j0sw} \\ &= (36\ \mu\text{m}^2 + 12\ \mu\text{m}^2) \cdot 0.095\ \text{fF}/\mu\text{m}^2 + 30\ \mu\text{m} \cdot 0.2\ \text{fF}/\mu\text{m} \\ &= 4.56\ \text{fF} + 6.0\ \text{fF} \\ &= 10.56\ \text{fF} \end{aligned}$$

The minimum value of the drain junction capacitance is achieved when the junction is biased (in reverse) with its maximum possible voltage, V_{max}. In order to calculate the minimum capacitance value, we first find V_{max} using (9.5), as follows.

$$\begin{aligned} V_{max} &= 5.0 - 0.8 - 0.4\left(\sqrt{0.6 + V_{max}} - \sqrt{0.6}\right) \\ \Rightarrow V_{max} &= 3.68\ \text{V} \end{aligned}$$

Now, the minimum value of the drain junction capacitance can be calculated.

$$\begin{aligned} C_{db,min} &= \frac{C_{bottom}}{\sqrt{1 + \dfrac{V_{x,max}}{\phi_0}}} + \frac{C_{sidewall}}{\sqrt{1 + \dfrac{V_{x,max}}{\phi_{0sw}}}} \\ &= \frac{4.56\ \text{fF}}{\sqrt{1 + \dfrac{3.68}{0.88}}} + \frac{6.0\ \text{fF}}{\sqrt{1 + \dfrac{3.68}{0.95}}} = 4.71\ \text{fF} \end{aligned}$$

The minimum value of the total soft-node capacitance is found by using (9.21).

$$\begin{aligned} C_{x,min} &= C_{gb} + C_{metal} + C_{poly} + C_{db,min} \\ &= 0.52\ \text{fF} + 0.90\ \text{fF} + 2.42\ \text{fF} + 4.71\ \text{fF} \\ &= 8.55\ \text{fF} \end{aligned}$$

The amount of the critical charge drop in the soft node, which will eventually cause a change of logic state, is

$$\begin{aligned} \Delta Q_{critical} &= C_{x,min} \cdot \left(V_{x,max} - \frac{V_{DD}}{2}\right) \\ &= 8.55\ \text{fF} \cdot (3.68\ \text{V} - 2.5\ \text{V}) \\ &= 10.09\ \text{fC} \end{aligned}$$

assuming that the logic threshold voltage of the next gate is $(V_{DD}/2)$. In this example, the maximum leakage current responsible for charge depletion is given from the MOS characteristics (cf. equation (3.92) in Chapter 3) and the junction diode characteristics as

$$I_{leakage} = I_{subthreshold} + I_{reverse} = 0.85\ \text{pA}$$

Finally, we calculate the worst-case (minimum) hold time for the soft node using the expression (9.22).

$$\begin{aligned} t_{hold,min} &= \frac{\Delta Q_{critical}}{I_{leakage,max}} \\ &= \frac{10.09\ \text{fC}}{0.85\ \text{pA}} = \underline{\underline{11.87\ \text{ms}}} \end{aligned}$$

It is interesting to note that even with a very small soft-node capacitance of 8.55 fF, the worst-case hold time for this structure is relatively long, especially compared with the signal propagation delays encountered in nMOS or CMOS logic gates. This example proves the feasibility of the dynamic charge storage concept and shows that a logic state can be preserved in a soft node for a long time period when the leakage current is small.

Voltage bootstrapping

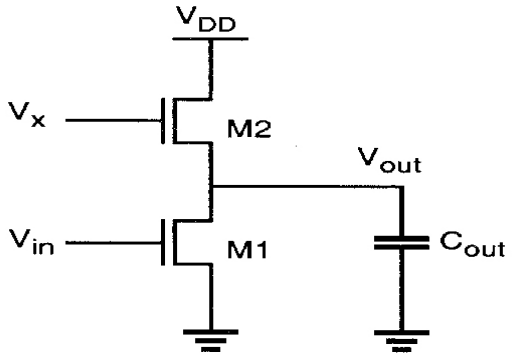


Figure 9.11 Enhancement-type circuit in which the output node is weakly driven.

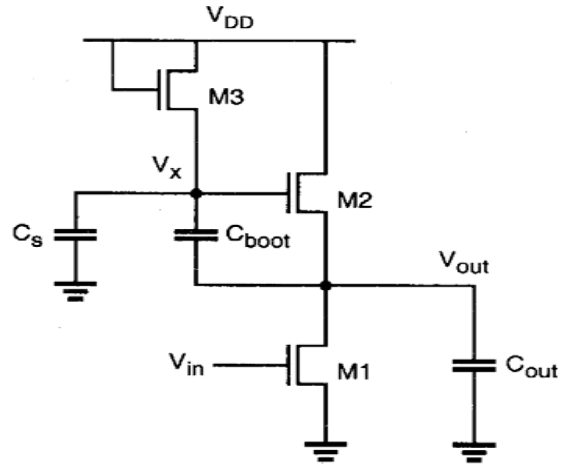


Figure 9.12 Dynamic bootstrapping arrangement to boost V_x during switching.

- *To overcome threshold voltage drops in digital circuits*
- *Figure 9.11*
  - *Considering $V_x \le V_{DD} \Rightarrow$ M2 in saturation , $V_{out(max)}=V_x-V_{T2(Vout)}$*
  - *To obtain a full logic-high level V_{DD}, the voltage V_x must be increased*
- *Figure 9.12*
  - *A third transistor has been added to the circuit*
  - *C_s: dynamic couple to the ground*
  - *C_{boot}: dynamic couple to V_x*
  - *This circuit produce a high V_x during switching*
    - *$V_x \ge V_{DD}+V_{T2}(V_{out})$*

Voltage bootstrapping

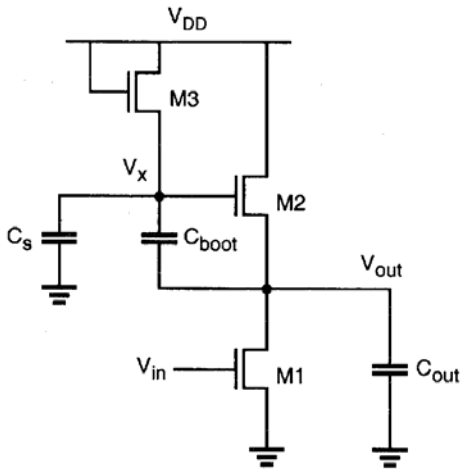


Figure 9.12 Dynamic bootstrapping arrangement to boost V_x during switching.

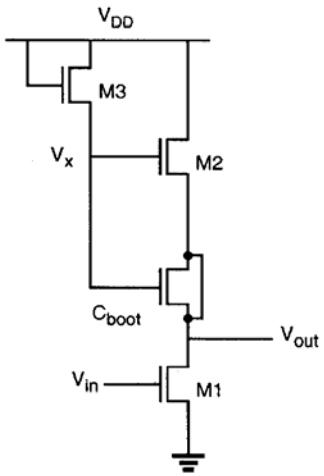


Figure 9.13 Realization of the bootstrapping capacitor with a dummy MOS device.

$$V_x = V_{DD} - V_{T3}(V_x)$$

$$i_{Cs} \approx i_{Cboot} \Leftrightarrow C_s \frac{dV_x}{dt} \approx C_{boot} \frac{d(V_{out} - V_x)}{dt}$$

$$(C_s + C_{boot})\frac{dV_x}{dt} \approx C_{boot}\frac{dV_{out}}{dt} \Rightarrow \frac{dV_x}{dt} \approx \frac{C_{boot}}{(C_s + C_{boot})}\frac{dV_{out}}{dt}$$

$$\int_{V_{DD}-V_{T3}}^{V_x} dV_x = \frac{C_{boot}}{(C_s + C_{boot})}\int_{V_{OL}}^{V_{DD}} dV_{out} \Rightarrow V_x = (V_{DD} - V_{T3}) + \frac{C_{boot}}{(C_s + C_{boot})}(V_{DD} - V_{OL})$$

if C_{boot} is much larger than $C_s \Rightarrow V_{x(\max)} = 2V_{DD}\text{-}V_{T3}\text{-}V_{OL}$

$$V_{x(\min)} = V_{DD} + V_{T2}\Big|_{V_{OUT}=V_{DD}} = (V_{DD} - V_{T3}(V_x)) + \frac{C_{boot}}{(C_s + C_{boot})}(V_{DD} - V_{OL})$$

$$\frac{C_{boot}}{(C_s + C_{boot})} = \frac{V_{T2}\Big|_{V_{OUT}=V_{DD}} + V_{T3}\Big|_{V_x}}{(V_{DD} - V_{OL})}$$

$$\frac{C_{boot}}{C_s} = \frac{V_{T2}\Big|_{V_{OUT}=V_{DD}} + V_{T3}\Big|_{V_x}}{V_{DD} - V_{OL} - V_{T2}\Big|_{V_{OUT}=V_{DD}} - V_{T3}\Big|_{V_x}}$$

*Cs: the sum of the parasitic source-to-substrate cap. ofM3 and the gate-to substrate cap of M2

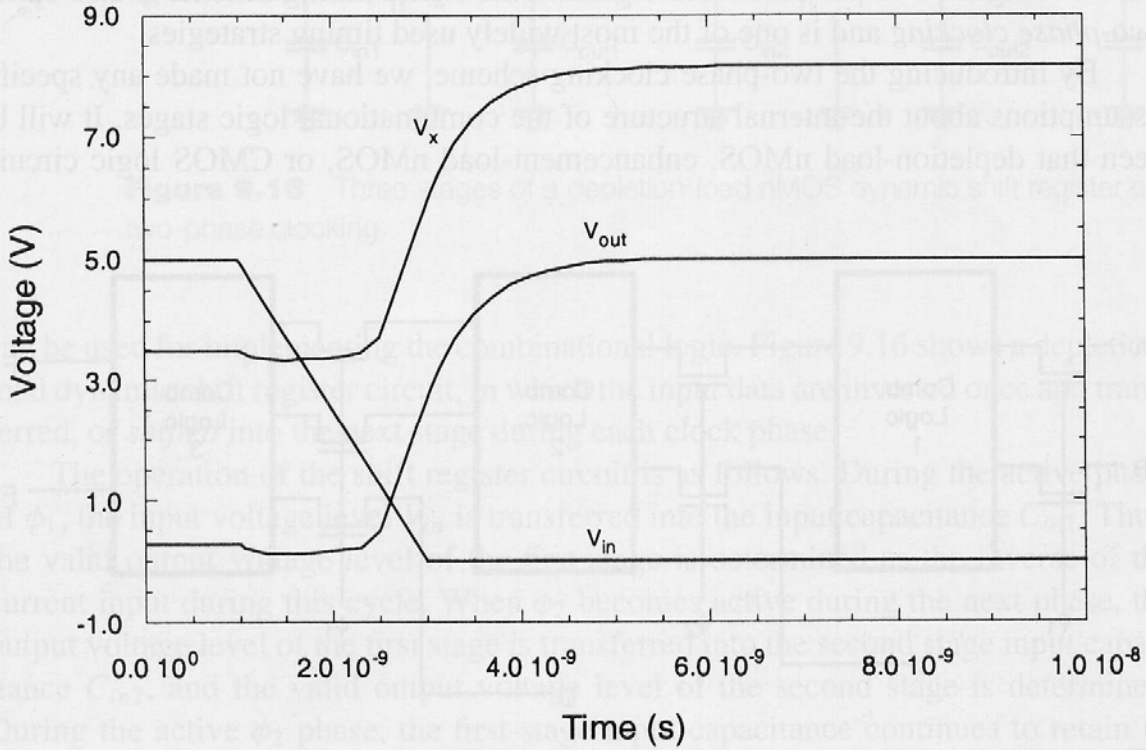
*To obtain a sufficiently large bootstrap cap. C_{boot} in comparison to C_s, an extra "dummy" transistor is added

*The dummy transistor acts as an MOS capacitor between V_x and V_{out}

Example 9.3

EXAMPLE 9.3

The transient operation of the simple bootstrap circuit shown in Fig. 9.13 is simulated using SPICE in the following. To provide the needed bootstrap capacitance C_{boot}, a dummy nMOS device with channel length $L = 5\ \mu$m and channel width $W = 50\ \mu$m is used. Transistor M1 has a (W/L) ratio of 2, while M2 and M3 each have a (W/L) ratio of 1.



Synchronous dynamic circuit techniques

- Previous section
  - Basic concepts associated with temporary storage of logic levels in capacitive circuit nodes
- This section
  - Pay attention to digital circuit design
  - Different examples of synchronous dynamic circuit
    - Depletion-load nMOS
    - Enhancement-load nMOS
    - CMOS building block

Dynamic pass transistor circuits

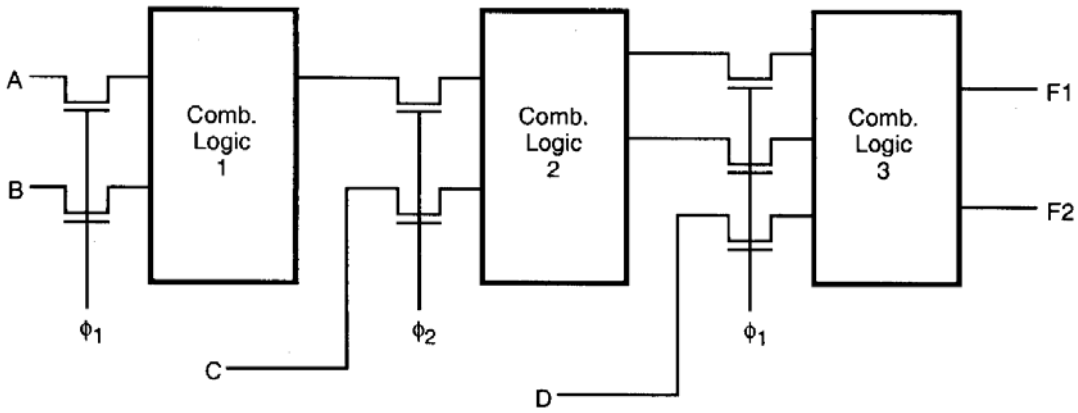


Figure 9.14 Multi-stage pass transistor logic driven by two nonoverlapping clocks.

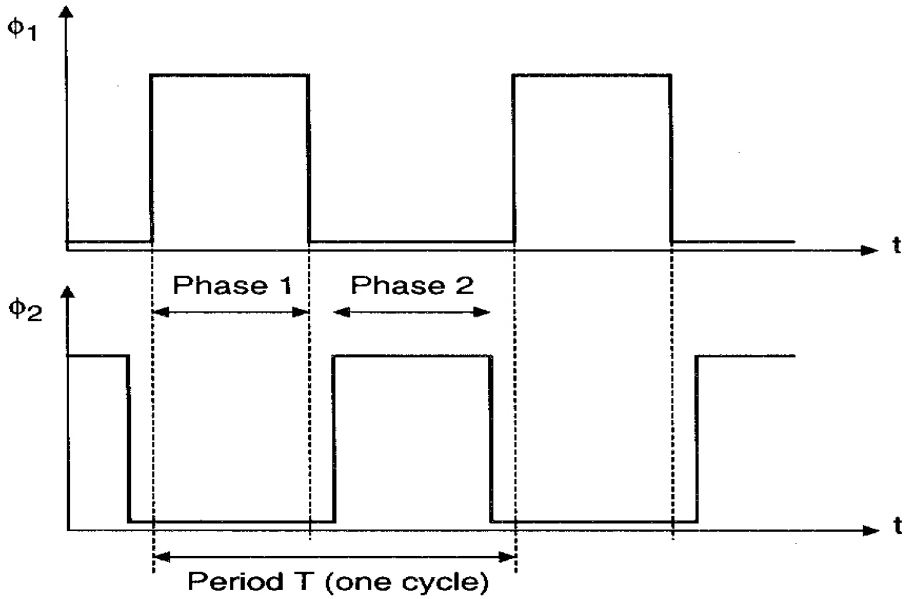


Figure 9.15 Nonoverlapping clock signals used for two-phase synchronous operation.

- *Cascaded combinational logic stage*
- *Interconnected through nMOS transistor*
- *All input of each combinational logic block are driven by a single clock signal*
- *Two phase clocking*

Depletion-load nMOS dynamic shift register circuit

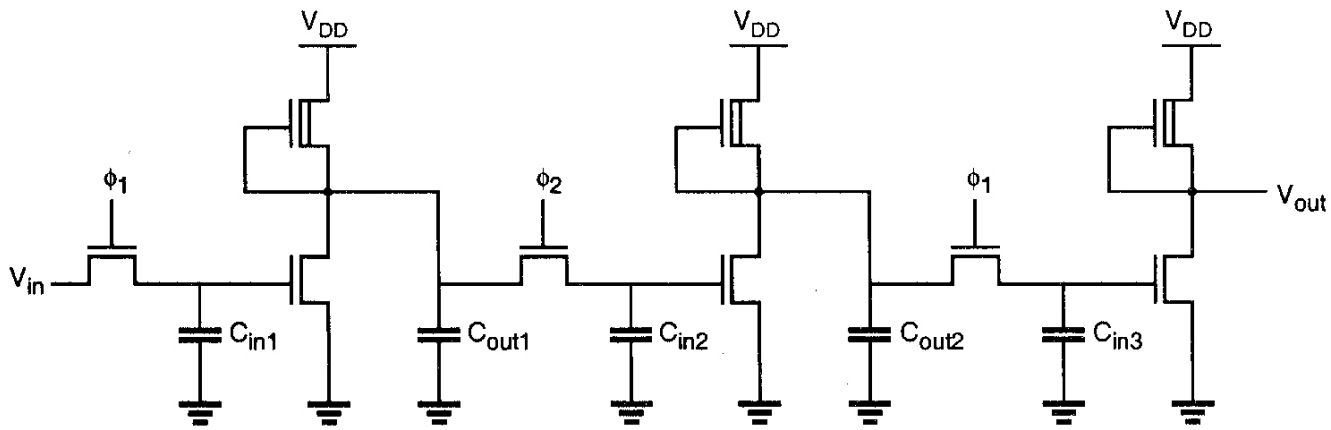


Figure 9.16 Three stages of a depletion-load nMOS dynamic shift register circuit driven with two-phase clocking.

- *Φ1 active*
  - *Vin is transferred to Cin1 ⇒ Vout1 is determined*
- *Φ2 active*
  - *Vout1 is transferred to Cin2 ⇒ Vout2 is determined*
  - *Cin1 retain its previous level via charge storage*
- *Φ1 active again*
  - *The original data bit written into the register (3rd)*
  - *!st stage accept new data*

Depletion-load nMOS dynamic shift register circuit

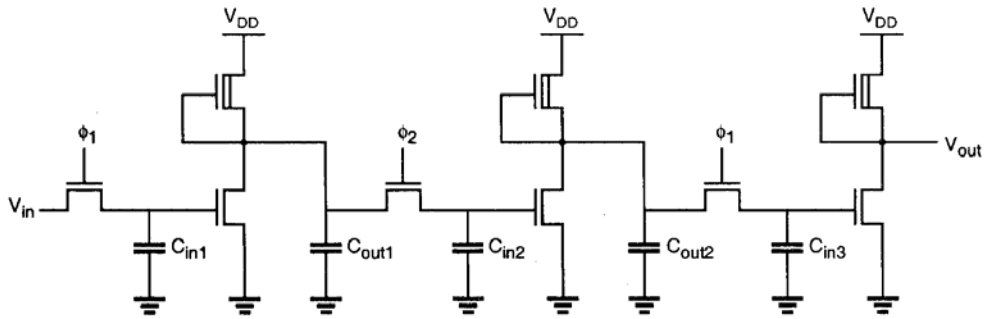


Figure 9.16 Three stages of a depletion-load nMOS dynamic shift register circuit driven with two-phase clocking.

- Maximum clock frequency
  - Being determined by
    - the signal propagation delay through one inverter stage
  - One half-period of the clock signal must be long enough to allow
    - Cin to charge up or down
    - and the logic level to propagate to the output by charging Cout
- Logic-high input level of each inverter stage is one threshold voltage lower than the power supply level

A two-stage synchronous complex logic circuit

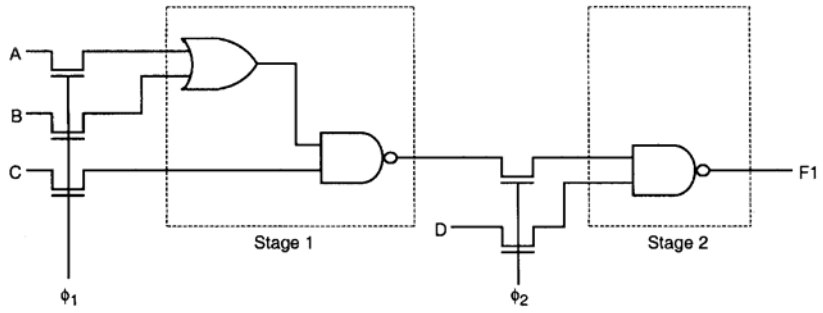


Figure 9.17 A two-stage synchronous complex logic circuit example.

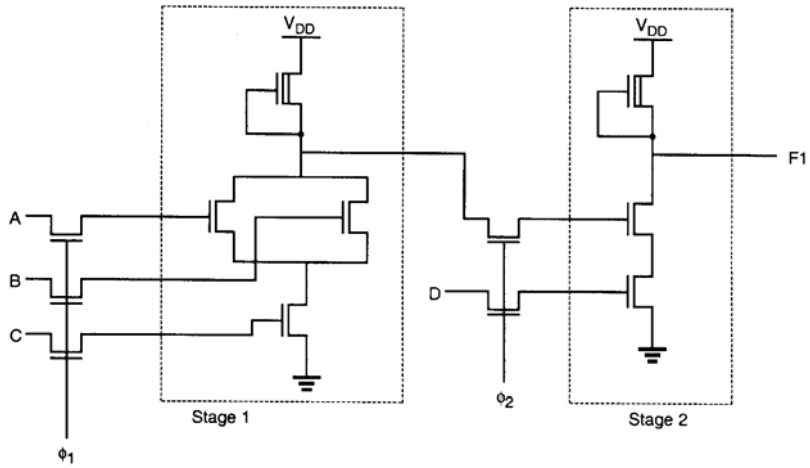


Figure 9.18 Depletion-load nMOS implementation of synchronous complex logic.

- *The same operation principle extended to synchronous complex logic*
- *In order to guarantee correct logic levels are propagated during each active clock cycle*
  - *The half period length of the clock signal must be longer than the largest signal-stage signal propagation delay found in the cirucit*

Enhancement-load dynamic shift register (ratioed logic)(1)

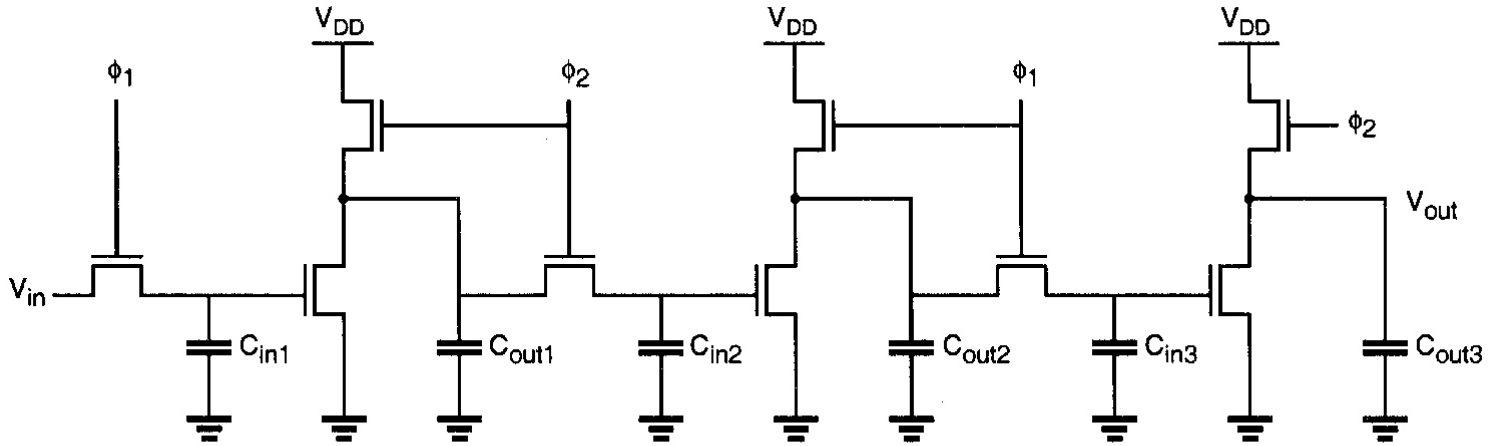


Figure 9.19 Enhancement-load dynamic shift register (ratioed logic).

- One important difference
  - Applying the clock signal to the gate of the load transistor
- Power dissipation and the silicon area can be reduced significantly
- The input pass transistor and load transistor are driven by opposite clock phase

Enhancement-load dynamic shift register (ratioed logic)(2)

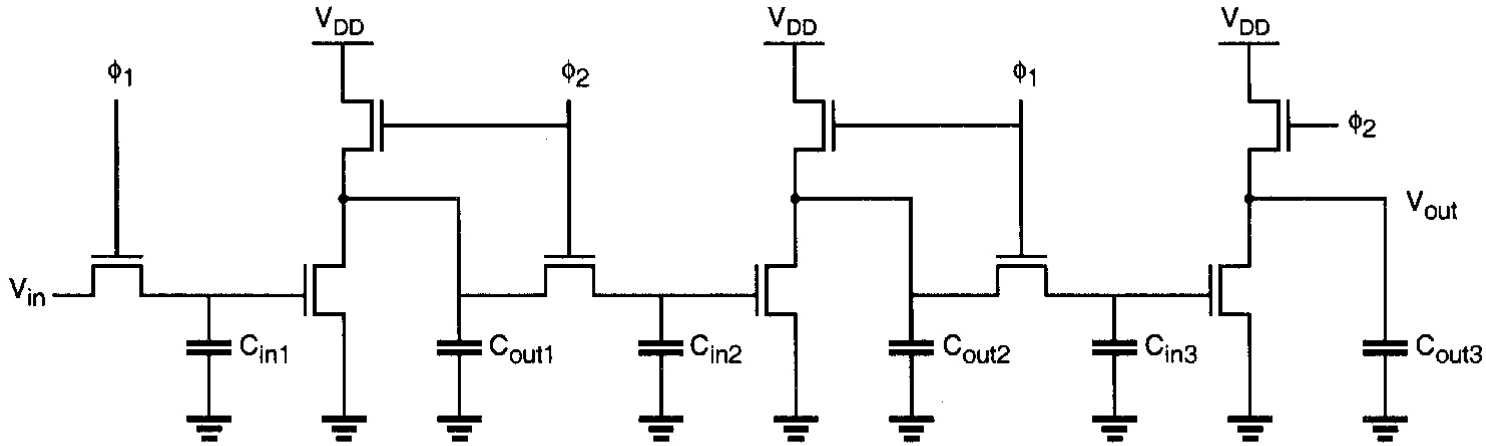


Figure 9.19 Enhancement-load dynamic shift register (ratioed logic).

- *Φ1 active*
  - *Vin ⇒ Cin1, nMOS load off*
- *Φ2 active*
  - *nMOS load on, the output of 1st inverter attains its valid logic (Cin1 preserved)*
  - *Pass transistor of 2nd stage on*
    - *Cout1 ⇒ Cin2*
- *Φ1 active*
  - *Cout2 is determined and transferred into Cin3*
  - *Also, a new input level can be accepted into Cin1*
- *V_{OL} of each stage is strictly determined by the driver to load ratio (ratioed-dynamic logic)*

General circuit structure of ratioed synchronous dynamic logic

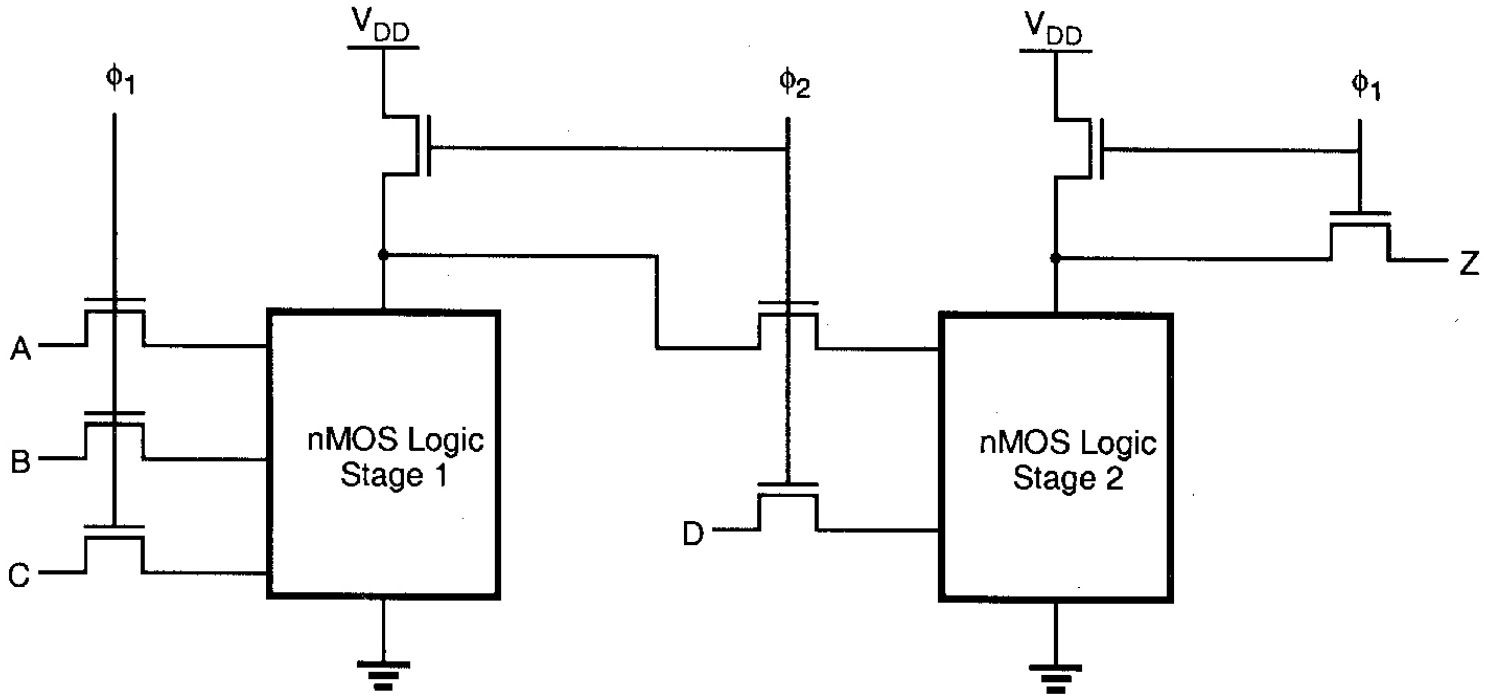


Figure 9.20 General circuit structure of ratioed synchronous dynamic logic.

- *Extended to arbitrary complex logic*

Enhancement-load dynamic shift register (ratioless logic)(1)

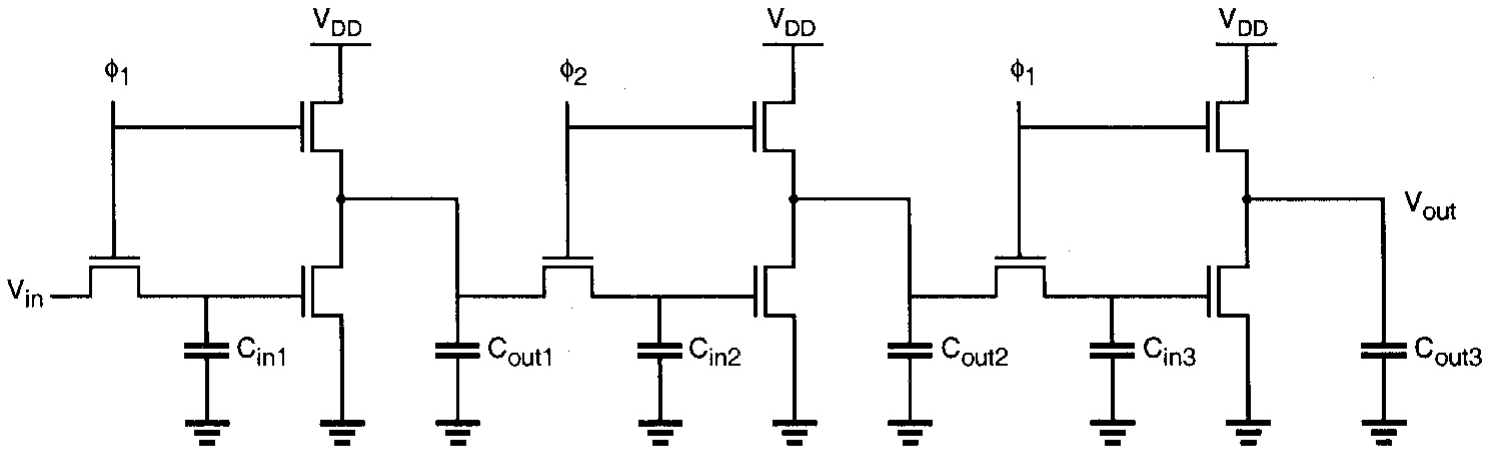


Figure 9.21 Enhancement-load dynamic shift register (ratioless logic).

- *In each stage, the input pass transistor and the load transistor are driven by the same clock phase*
- *Φ1 active*
  - *Vin transfer to Cin ⇒ 1st inverter is active ⇒ Vout1 attains its valid logic level*
- *Φ2 active*
  - *2nd pass transistor on ⇒ the logic level is transferred onto the next stage*

Enhancement-load dynamic shift register (ratioless logic)(2)

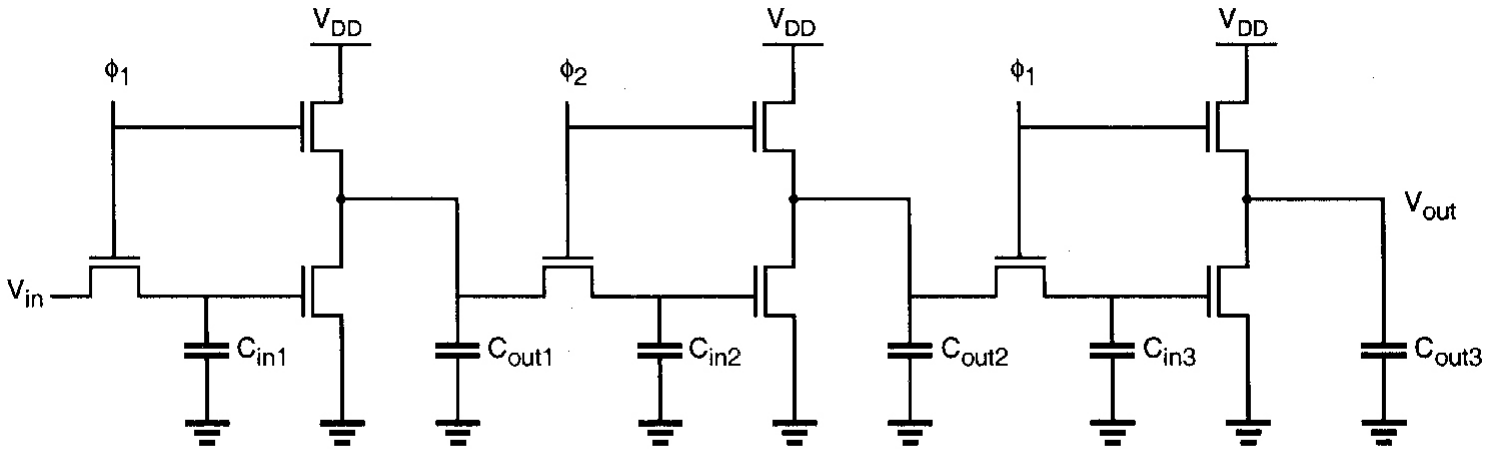


Figure 9.21 Enhancement-load dynamic shift register (ratioless logic).

- *Considering two cases*
  - *Case 1*
    - *If Cout1 high at the end of the active Φ1 phase*
      - *By mean of Cin1 low input ⇒ nMOS driver off ⇒Vout1=VDD-VTn*
    - *Φ2 active*
      - *The voltage level is transfer to Cin2 via charge sharing over the pass transistor*
      - *Cout/Cin ↑ to correctly transfer a logic-high level*

Enhancement-load dynamic shift register (ratioless logic)(3)

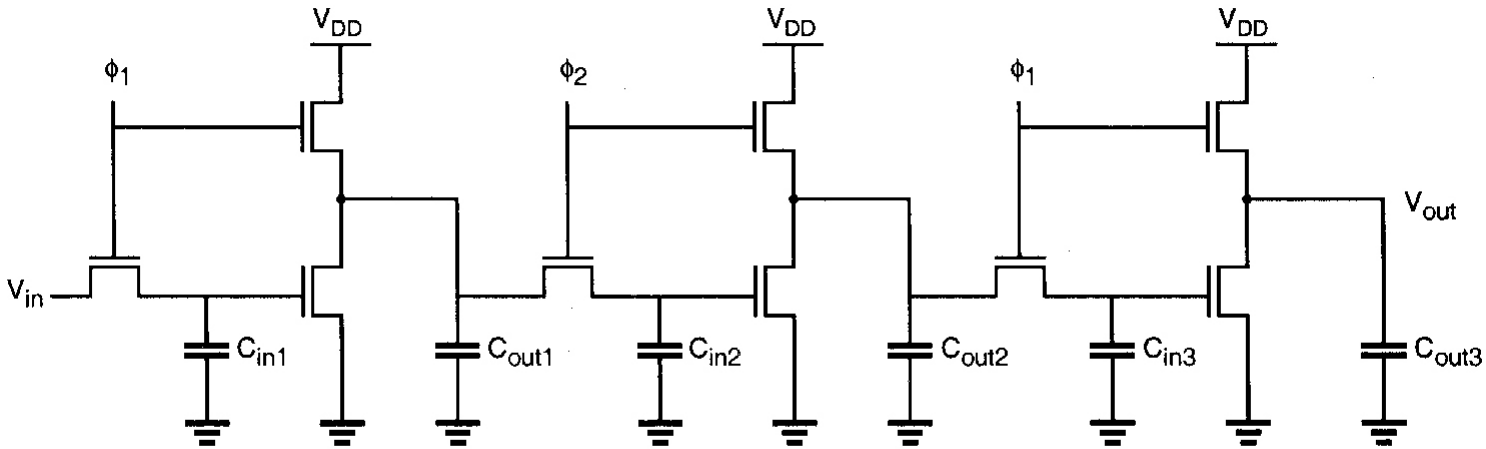


Figure 9.21 Enhancement-load dynamic shift register (ratioless logic).

- *Considering two cases*
  - *Case 2*
    - *If Vout1 is logic-low at the end of the active Φ1 phase*
      - *Cin1 high, nMOS driver on⇒ Vout1=0V*
    - *As Φ2 active*
      - *Transfer by pass transistor*
    - *Ratioless dynamic logic*
      - *V_{OL}=0, independent of driver-to-load ratio*

General circuit structure of ratioless synchronous dynamic logic

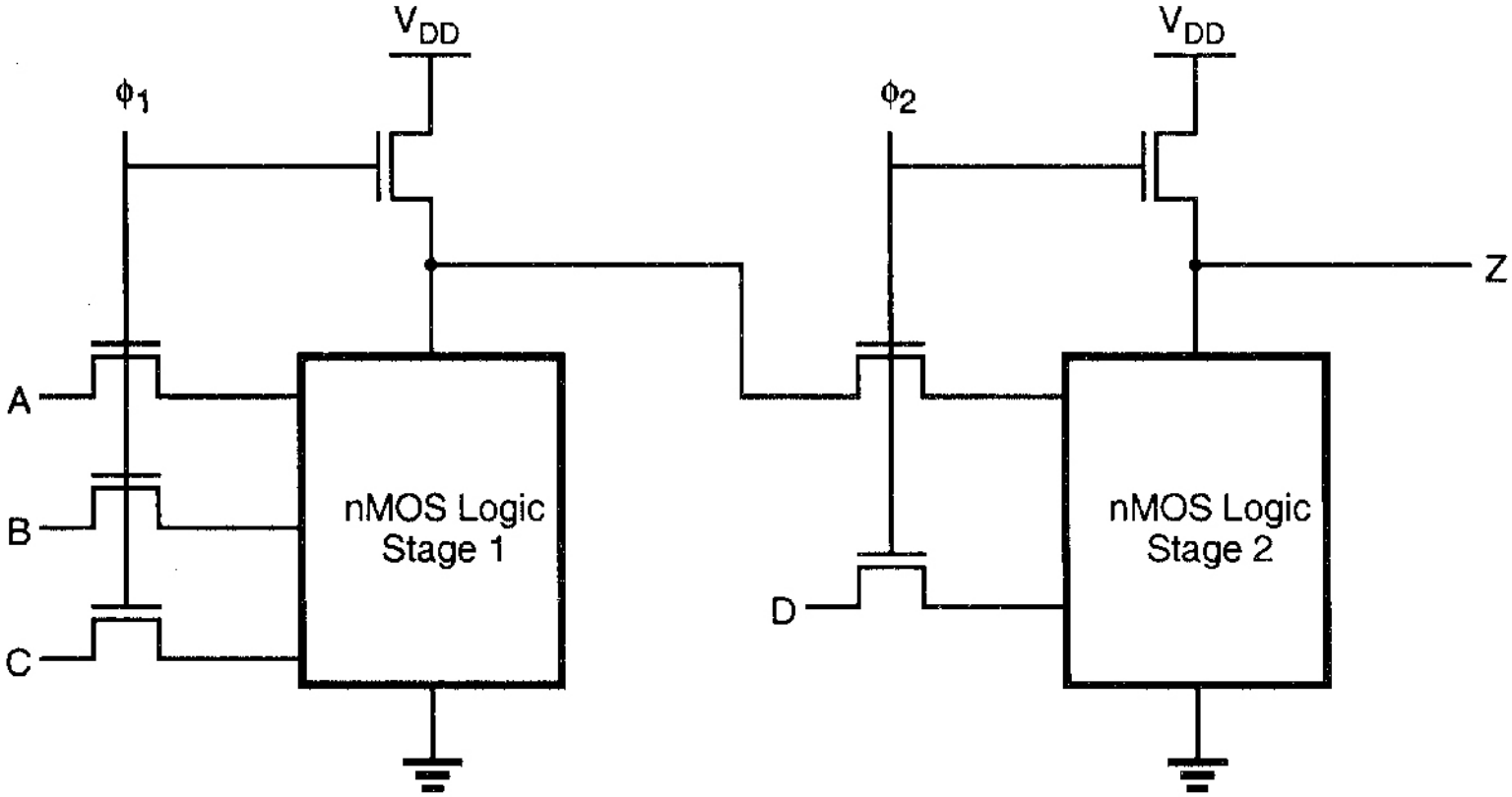


Figure 9.22 General circuit structure of ratioless synchronous dynamic logic.

Dynamic CMOS transmission gate logic

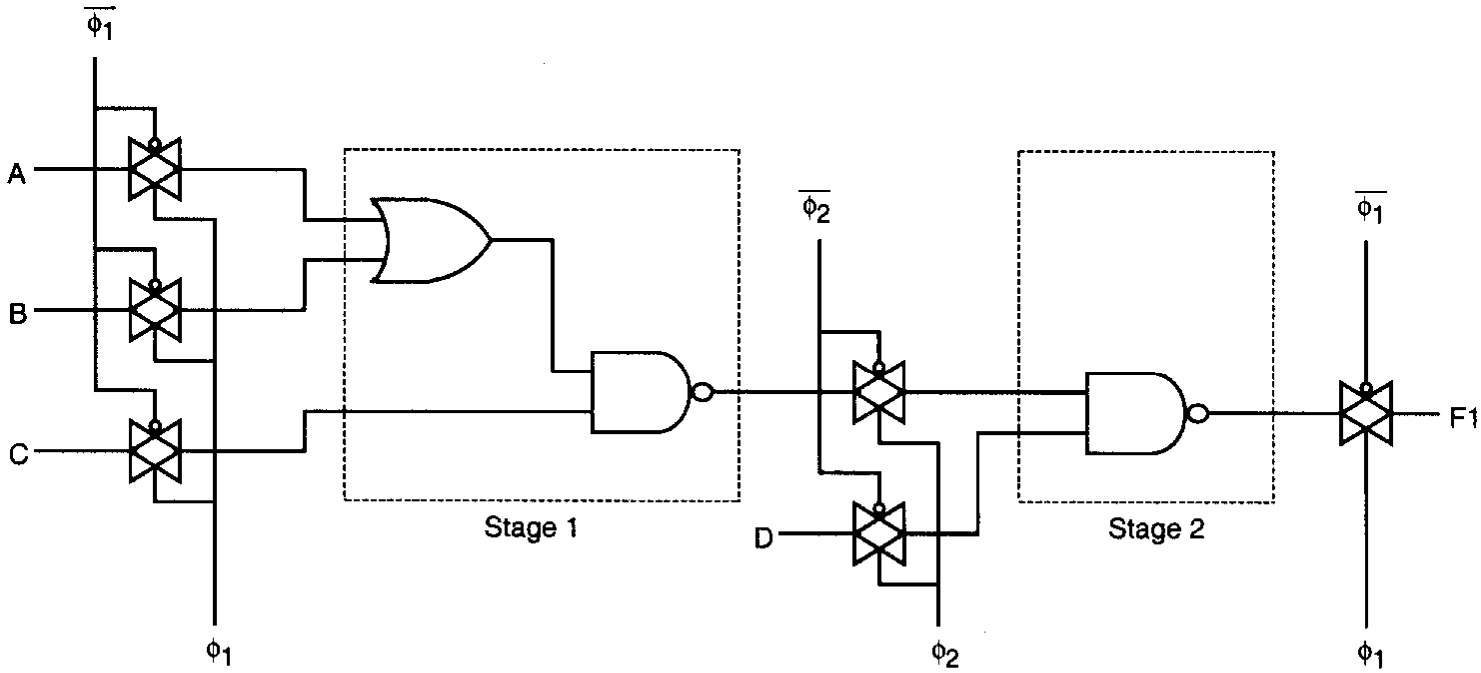


Figure 9.23 Typical example of dynamic CMOS transmission gate logic.

- *Totally, require four clock signals*

CMOS transmission gate dynamic shift register

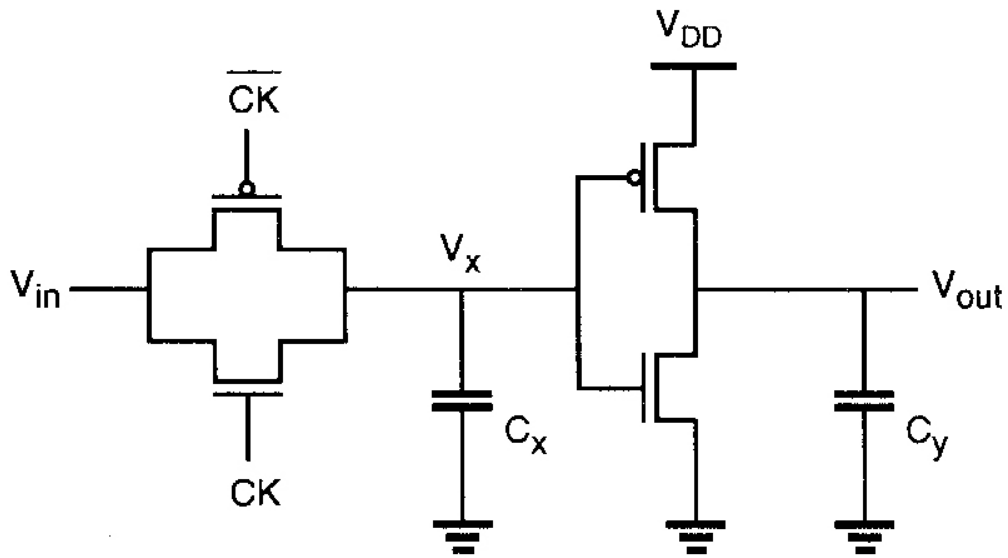


Figure 9.24 Basic building block of a CMOS transmission gate dynamic shift register.

- *Low on-resistance of transmission gate (ref.p310)*
  - *Smaller transfer time (RC↓)*
- *No threshold voltage drop*

Single-phase CMOS transmission gate dynamic shift register

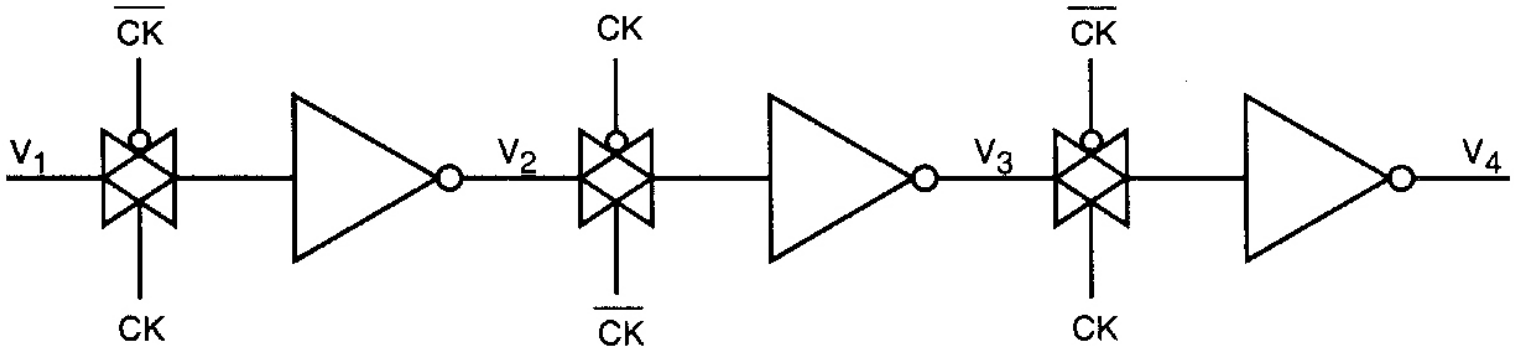


Figure 9.25 Single-phase CMOS transmission gate dynamic shift register.

- *Ideally, CK=1*
  - *Odd on, even off⇒ isolated*
- *In practical, do not truly nonoverlapping*
  - *CLK have finite t_r and t_f*
  - *So, prefer Φ1, Φ2*

Dynamic CMOS logic gate implementing a complex Boolean function(1)

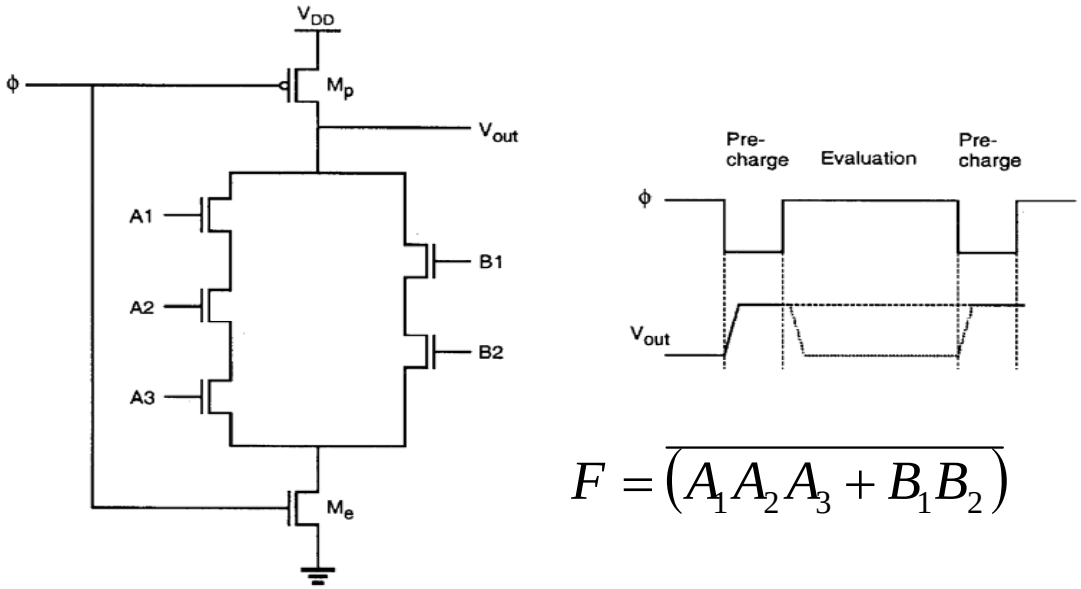


Figure 9.26 Dynamic CMOS logic gate implementing a complex Boolean function.

- *Significantly reduce the number of transistors used to implement any logic function*
- *Operation*
  - *First precharging the output node capacitance*
  - *Evaluating the output level according to the applied inputs*
  - *Both of theses of operations are scheduled by a single clock signal*
    - *Which drives one nMOS and one pMOS transistor in each dynamic stage*

Dynamic CMOS logic gate implementing a complex Boolean function(2)

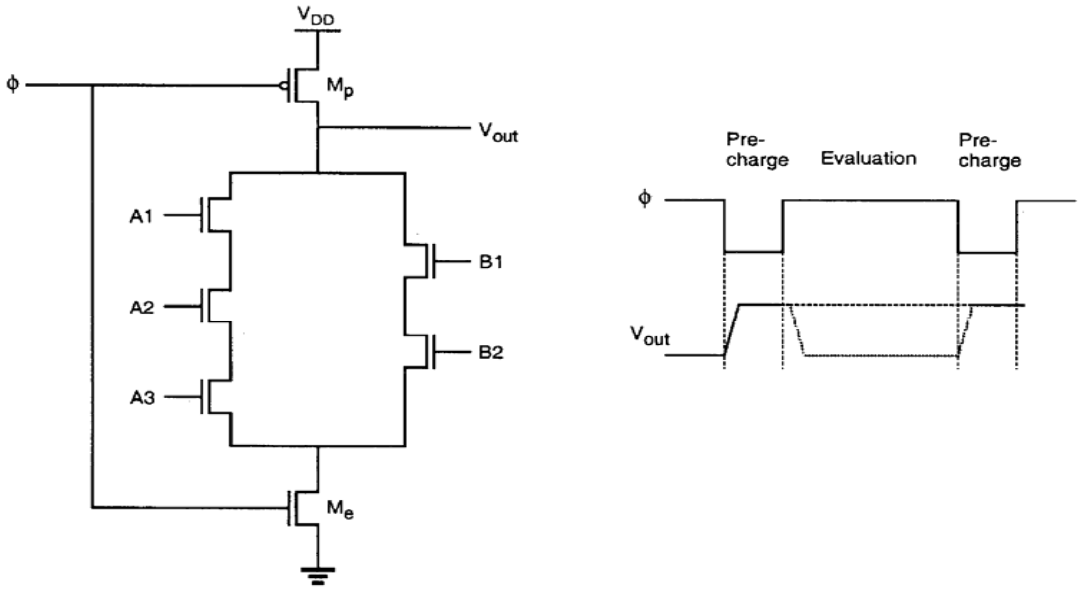


Figure 9.26 Dynamic CMOS logic gate implementing a complex Boolean function.

- *Φ=0 (precharge phase)*
  - *Mp on, Me off ⇒ the parasitic capacitance of the circuit is charged up to Vout=VDD*
    - *The input voltages are also applied during this phase⇒ no influence on the output*
- *Φ=1 (evaluate phase)*
  - *Mp off, Me on ⇒ the output voltage depend on the input voltage levels*
    - *VOL or VDD*
- *The practical multi-stage applications, however, the dynamic CMOS gate presents a significant problem*

Illustration of the cascading problem in dynamic CMOS logic(1)

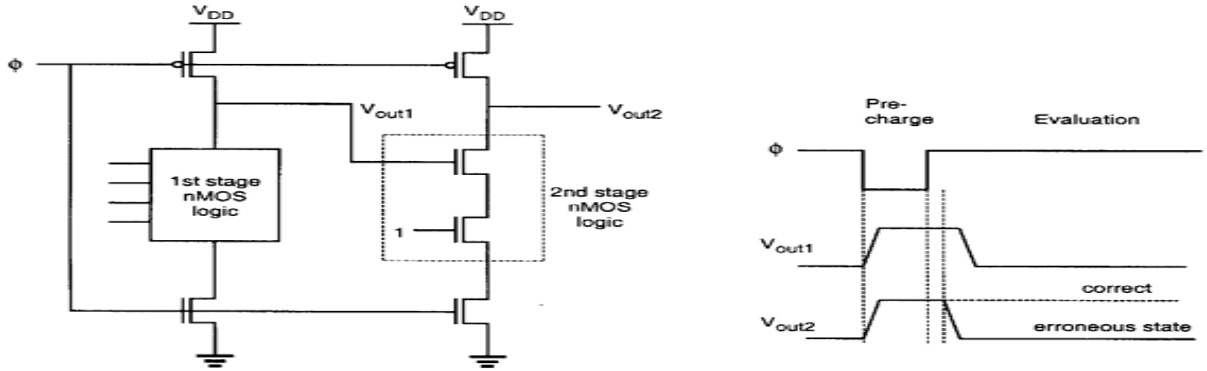


Figure 9.27 Illustration of the cascading problem in dynamic CMOS logic.

- *Assume*
  - *During the precharge phase*
    - *Both output voltages Vout1 and Vout2 are pulled up*
  - *During evaluation phase*
    - *The input variables of 1st stage assume to be such that*
      - *Output Vout1 drop to logic "0"*
    - *The external input of 2nd stage assume to be logic '1'*
- *As evaluation*
  - *Beginning*
    - *Both Vout1 an d Vout2 are logic-high*
  - *Then*
    - *Vout1 drops to its correct logic after a certain time delay*
    - *Vout2*
      - *Starting with the high value of Vout1 at the beginning of the evaluation phase, the output voltage Vout2 at the end of the evaluation phase will be erroneously low*

Illustration of the cascading problem in dynamic CMOS logic(1)

- This example illustrates that
  - Dynamic CMOS logic gates driven by the same clock signal cannot be cascade directly
  - This limitation undermine some advantages, such as
    - Low power dissipation
    - Large noise margins
    - Low transistor count

High-performance dynamic CMOS circuits

- Base on the basic dynamic CMOS logic gate structure
- Design to take full advantage of the obvious benefits of dynamic operation
- To all unrestricted cascading of multiple stages
- The ultimate goal is to achieve…,using the least complicated clocking scheme possible
  - Reliable
  - High-speed
  - Compact circuit

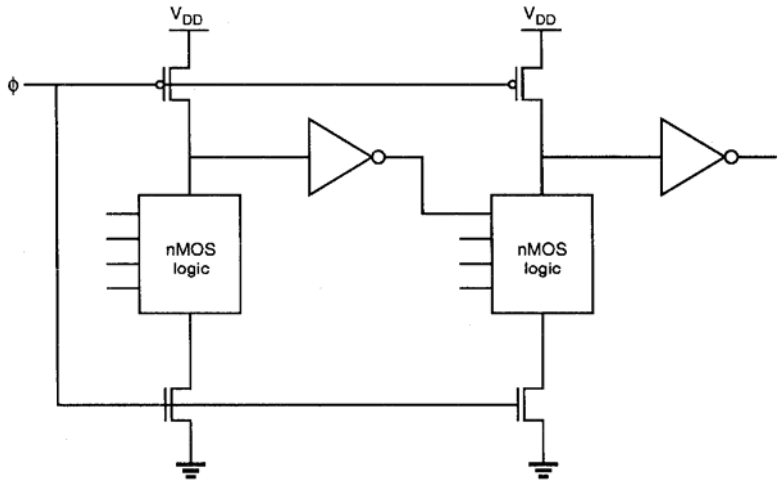


Figure 9.29 Cascaded domino CMOS logic gates.

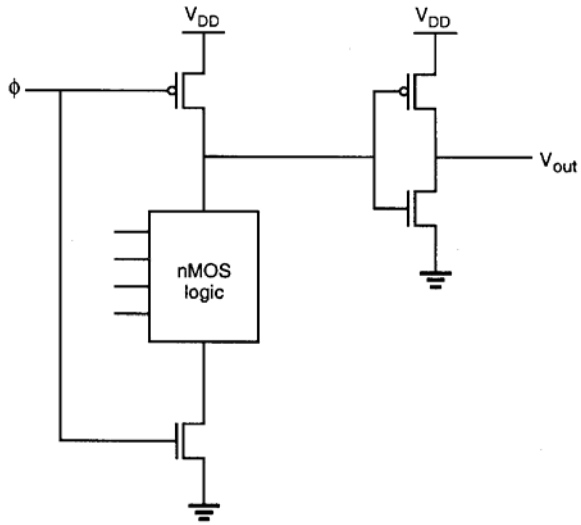


Figure 9.28 Generalized circuit diagram of a domino CMOS logic gate.

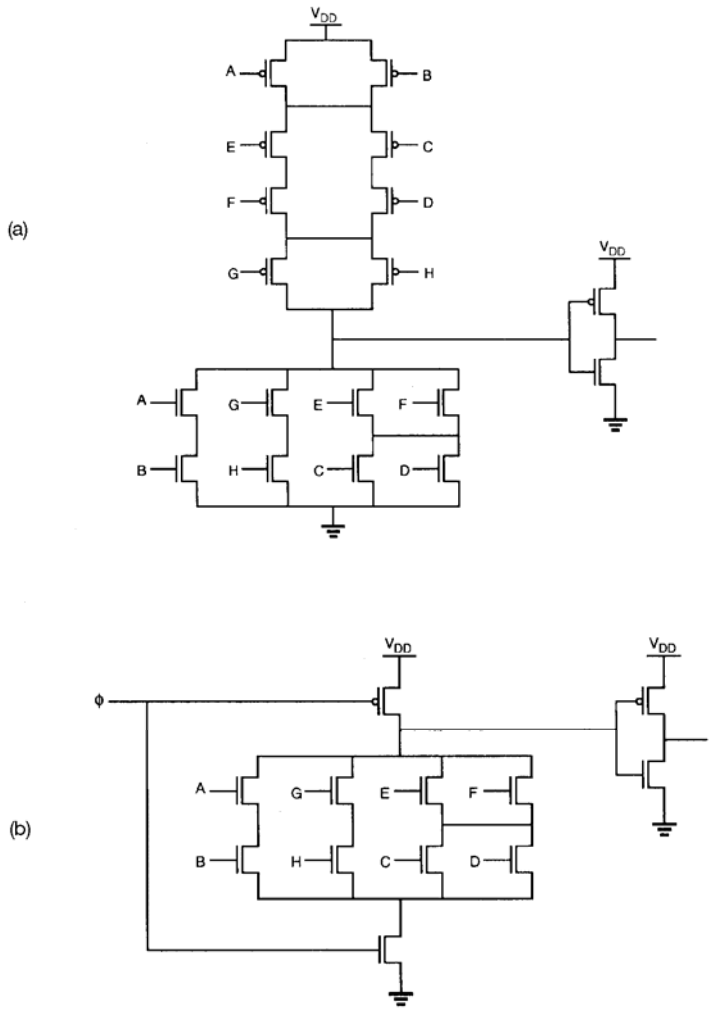


Figure 9.30 (a) An 8-input complex logic gate, realized using conventional CMOS logic and (b) domino CMOS logic.

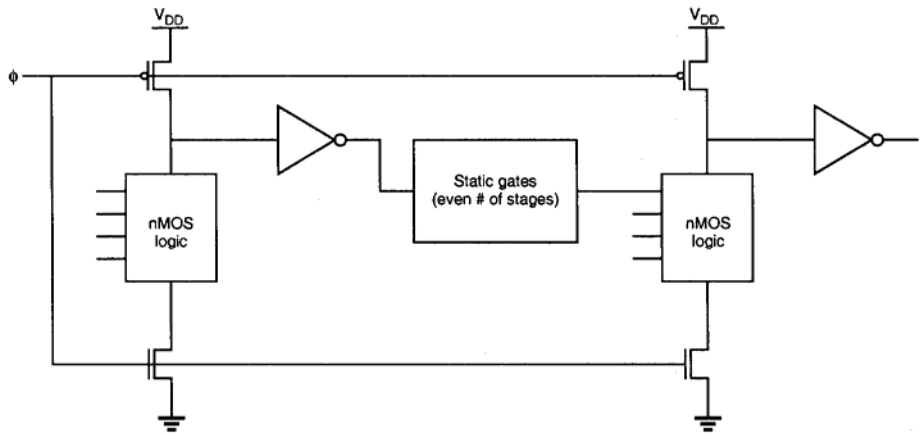


Figure 9.31 Cascading domino CMOS logic gates with static CMOS logic gates.

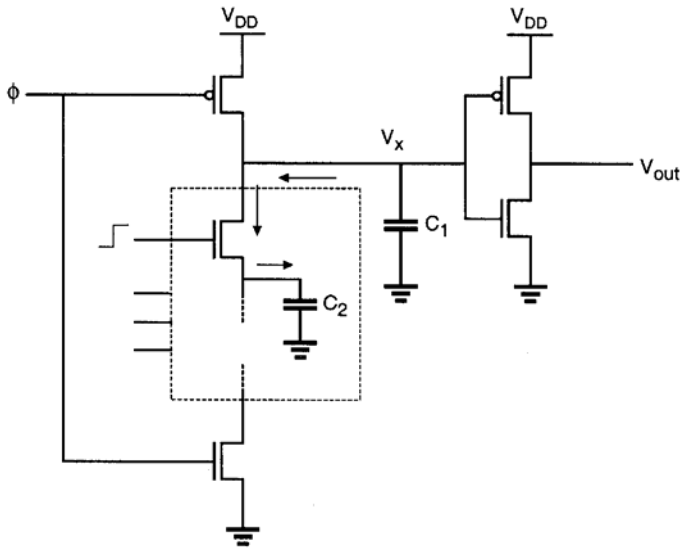


Figure 9.32 Charge sharing between the output capacitance C_1 and an intermediate node capacitance C_2 during the evaluation cycle may reduce the output voltage level.

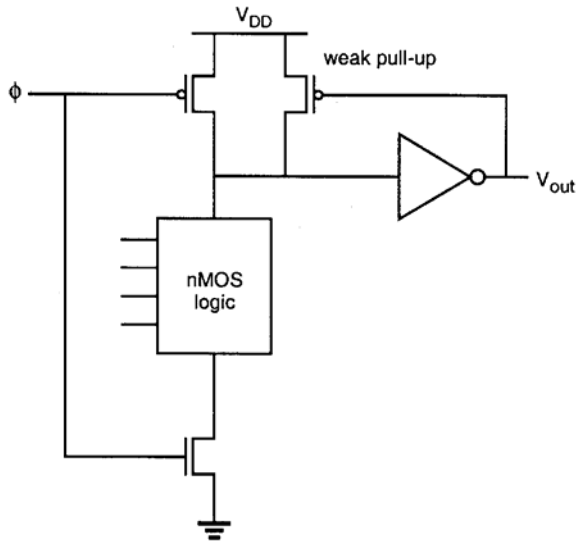


Figure 9.33 A weak pMOS pull-up device in a feedback loop can be used to prevent the loss of output voltage level due to charge sharing.

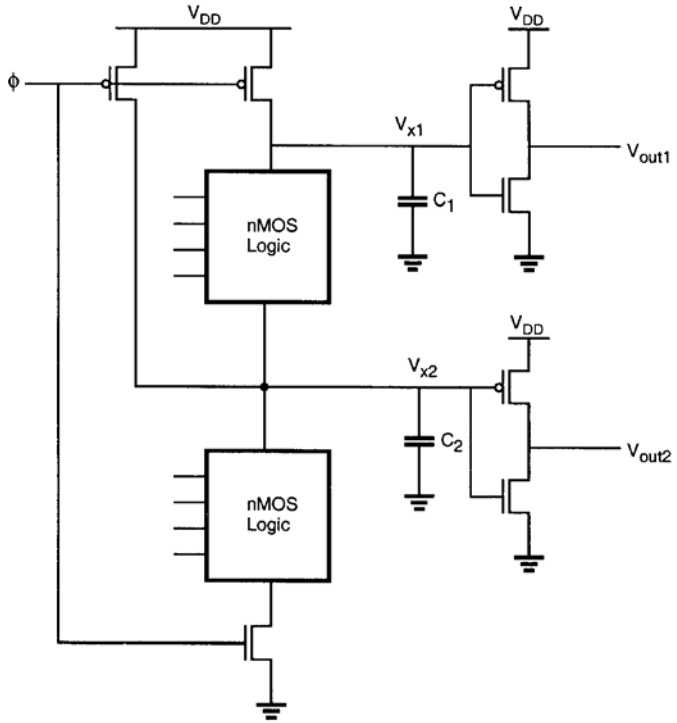


Figure 9.34 Precharging of internal nodes to prevent charge sharing also allows implementation of multiple-output domino CMOS structures.

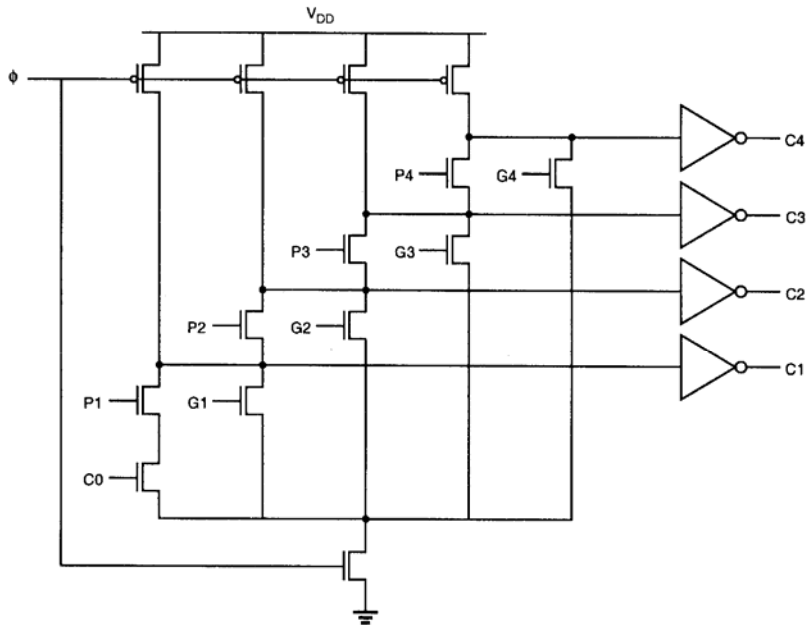


Figure 9.35 Example of a multiple-output domino CMOS gate realizing four functions.

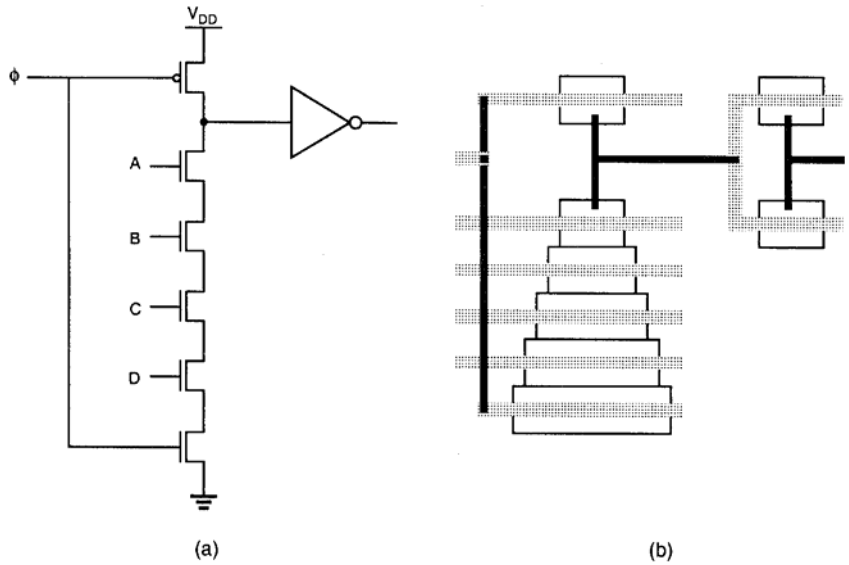
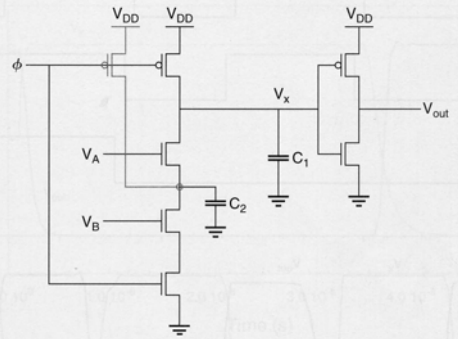


Figure 9.36 (a) Four-input domino CMOS NAND gate and (b) the corresponding stick-diagram layout to show the graded scaling of nMOS transistor sizes for improving the transient performance.

EXAMPLE 9.4

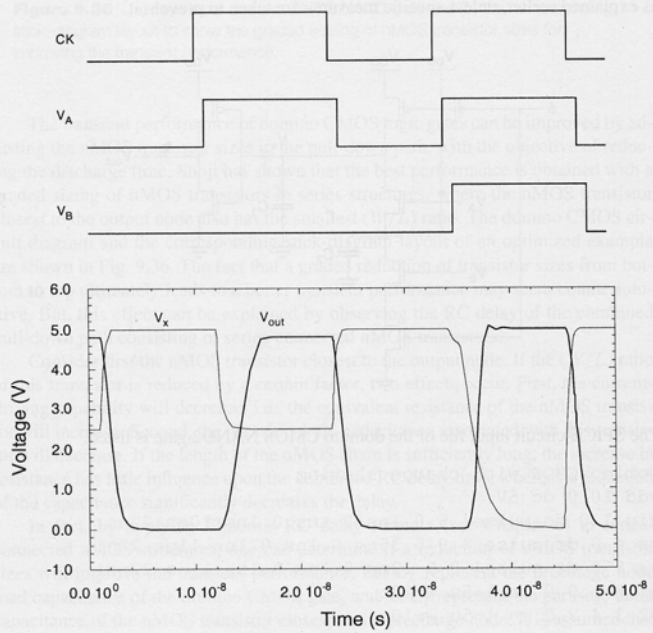
Consider the domino CMOS NAND2 gate shown below, where $C_1 = C_2 = 0.05$ pF. First, the operation of the circuit with only one pMOS precharge transistor will be examined. Since the two capacitances C_1 and C_2 are assumed to be equal to each other, we expect that the charge-sharing phenomenon will cause erroneous output values, as explained earlier, unless specific measures are taken to prevent it.



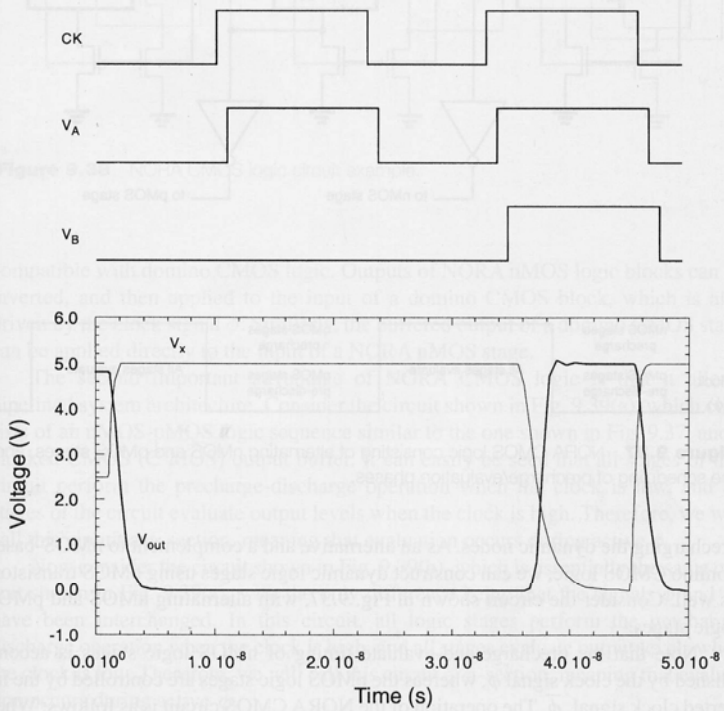
The SPICE-circuit input file of the domino CMOS NAND2 gate is listed.

```
Domino CMOS with charge sharing
vdd 10 0 dc 5V
vin 1 0 dc pulse( 5 0 1ns 0.1ns 0.1ns 10ns 22ns)
vb 4 0 dc pulse ( 0 5 35ns 0.1ns 0.1ns 11ns 22n)
va 5 0 dc pulse( 0 5 12ns 0.1ns 0.1ns 11ns 22ns)
m1 2 1 0 0 mn l=5u w=10u
m2 3 4 2 0 mn l=5u w=10u
m3 6 5 3 0 mn l=5u w=10u
m4 6 1 10 10 mp l=5u w=25u
m6 7 6 0 0 mn l=5u w=10u
m7 7 6 10 10 mp l=5u w=100u
cload 6 0 0.05p
cs 3 0 0.05p
cout 7 0 0.1p
.model mn nmos vto=1 gamma=0.4 kp=2.5e-5
.model mp pmos vto=-1 gamma=0.4 kp=1.0e-5
.tran 0.1ns 50ns
.print tran v(1) v(6) v(7) v(3)
.end
```

The transient simulation of this circuit shows that the precharge node voltage V_x drops to about 2.5 V during the evaluation phase, due to charge sharing. As a result, the inverter output voltage erroneously switches to logic-high level during the first evaluation phase.



Now consider the case where an additional pMOS precharge transistor is connected between the power supply voltage V_{DD} and the intermediate node, as indicated in the circuit diagram on page 391. Both pMOS transistors conduct during the precharge phase, and charge up the node capacitances to the same voltage level. Consequently, charge sharing can no longer cause a logic error at the output node. The simulation results *with* the additional pMOS precharge transistor are plotted below, showing that the output node voltage is pulled up to logic "1" only when both inputs are equal to logic "1."



It must be emphasized that there is a speed penalty for adding another pMOS precharge transistor to the circuit. Simulation results indicate that the pull-down delay of the node voltage V_x is actually increased by about 1 ns (approx. 25 percent) as a result of the additional parasitic capacitance which is due to the precharge device.

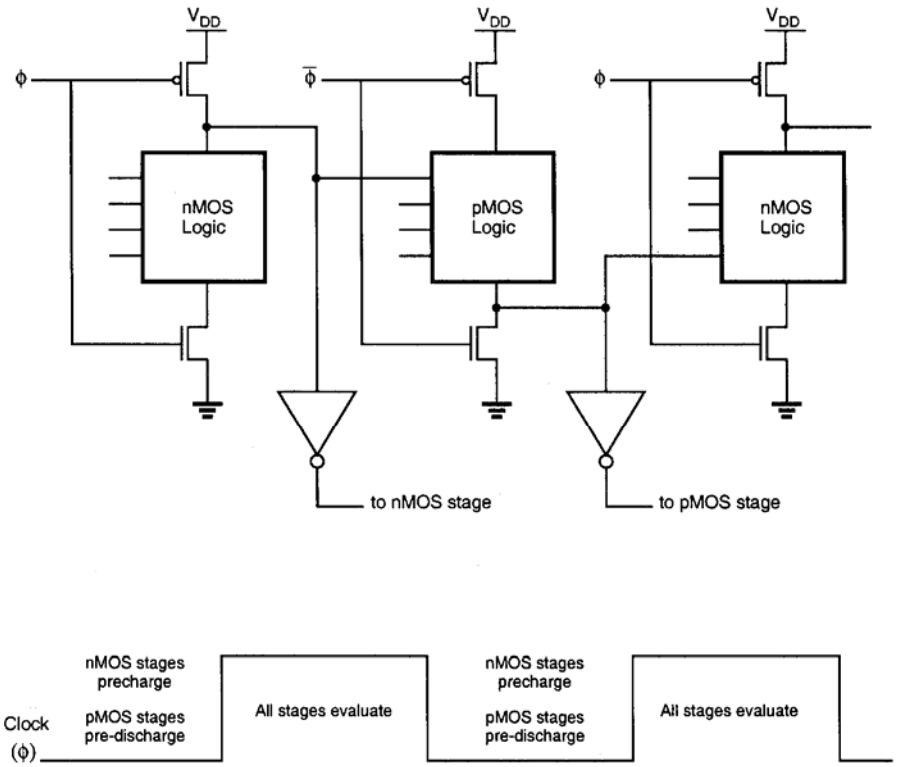


Figure 9.37 NORA CMOS logic consisting of alternating nMOS and pMOS stages, and the scheduling of precharge/evaluation phases.

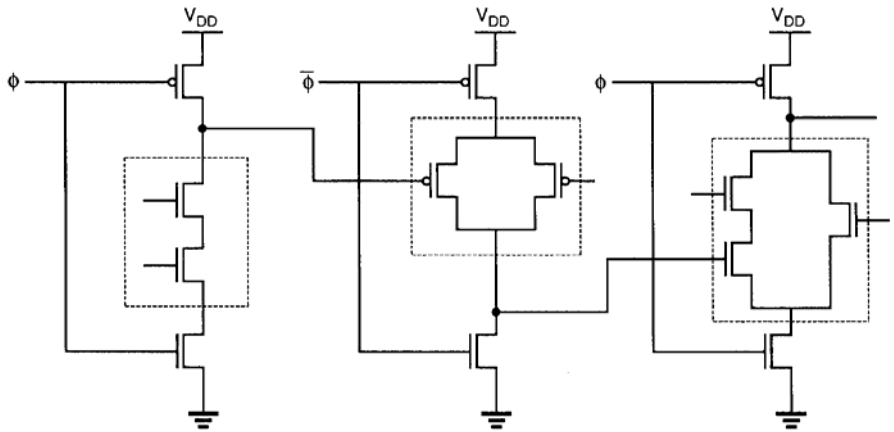


Figure 9.38 NORA CMOS logic circuit example.

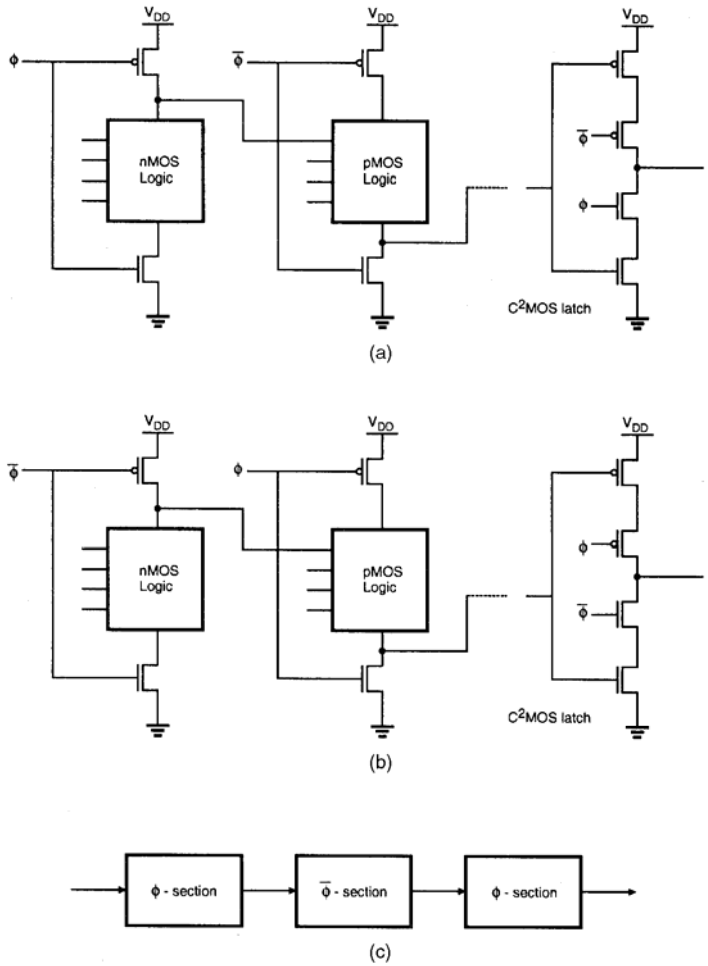


Figure 9.39 (a) NORA CMOS ϕ-section; evaluation occurs during $\phi = 1$. (b) NORA CMOS ϕ-section; evaluation occurs during $\phi = 0$. (c) A pipelined NORA CMOS system.

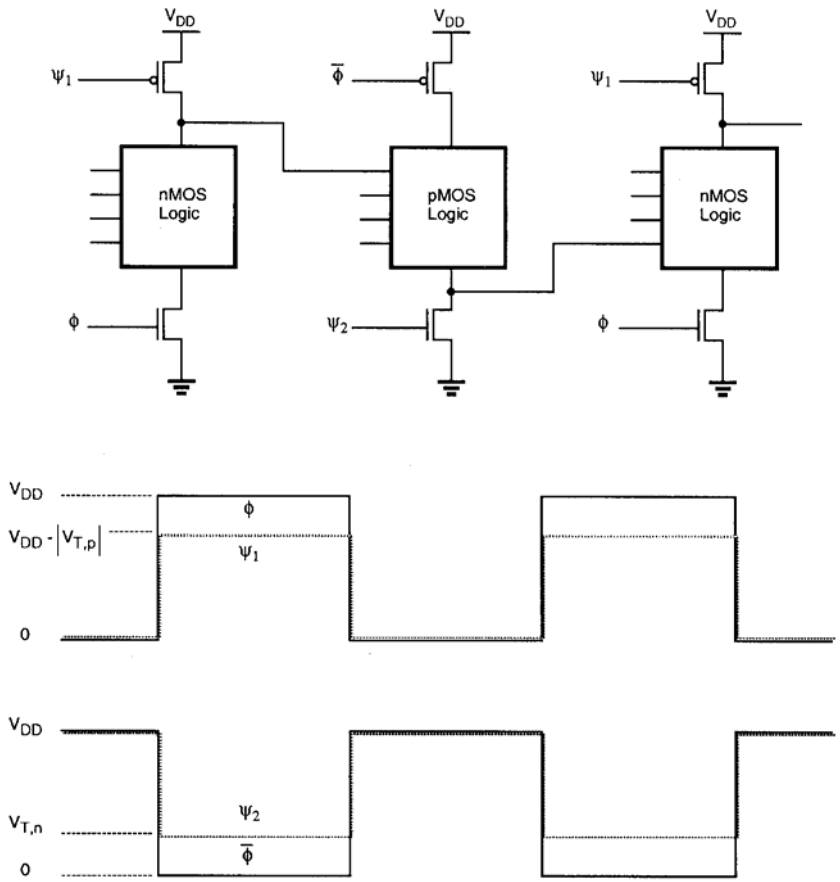


Figure 9.40 General circuit structure and the clock signals of Zipper CMOS.

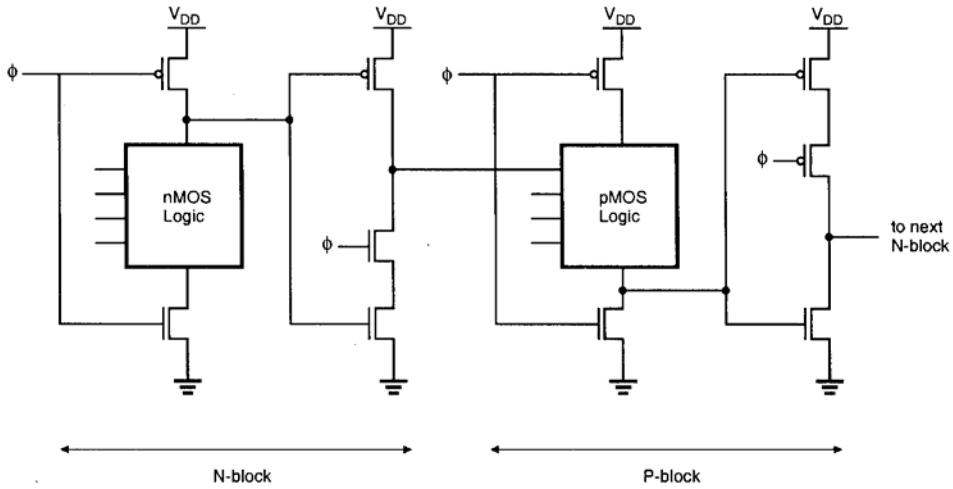


Figure 9.41 A pipelined true single-phase clock CMOS system.

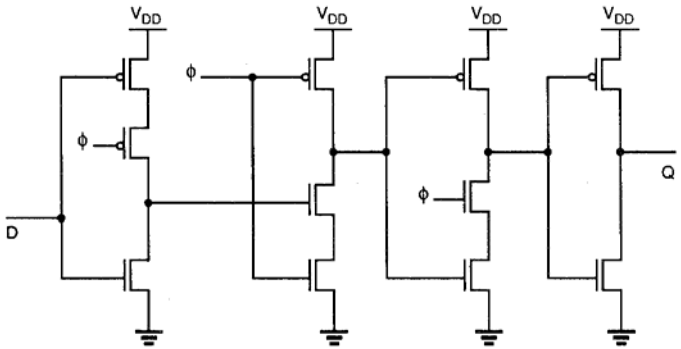


Figure 9.42 Circuit diagram of a TSPC-based rising edge-triggered DFF.

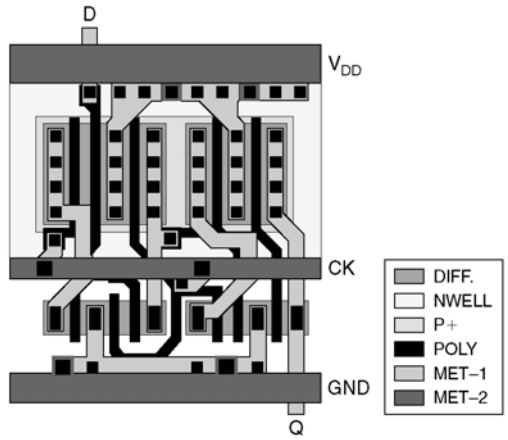


Figure 9.43 Mask layout of the TSPC-based DFF circuit.

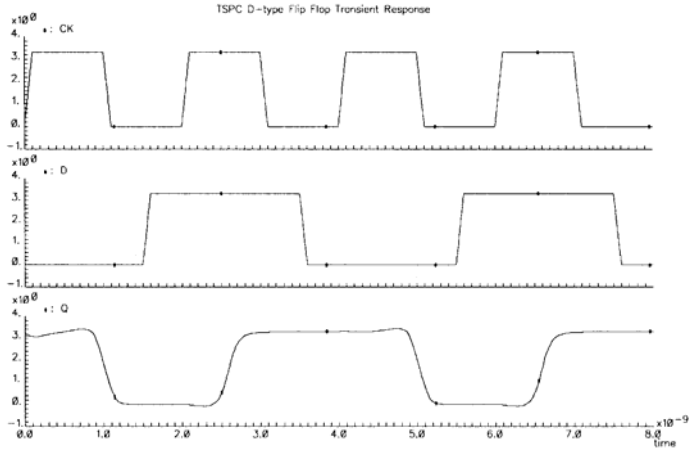


Figure 9.44 Simulation results showing the operation of the TSPC-based DFF circuit, with a clock frequency of 500 MHz.