CMOS

Digital Integrated Circuits

Analysis and Design

Chapter 8

Sequential MOS Logic Circuits

Introduction

- Combinational logic circuit
  - Lack the capability of storing any previous events
  - Non-regenerative circuit
    - There is no feedback relationship between the output and the input
- Sequential circuits
  - The output is determined by the current inputs as well as the previously applied input variables
  - Regenerative circuit
    - Bistable circuits
      - Two stable states
      - Most widely used and important
      - All basic latch, flip-flop circuits, registers, and memory elements
    - Monostable circuits
      - Only one stable operating point
    - Astable circuits
      - No stable operating point
      - Oscillate, without settling into a stable operating mode

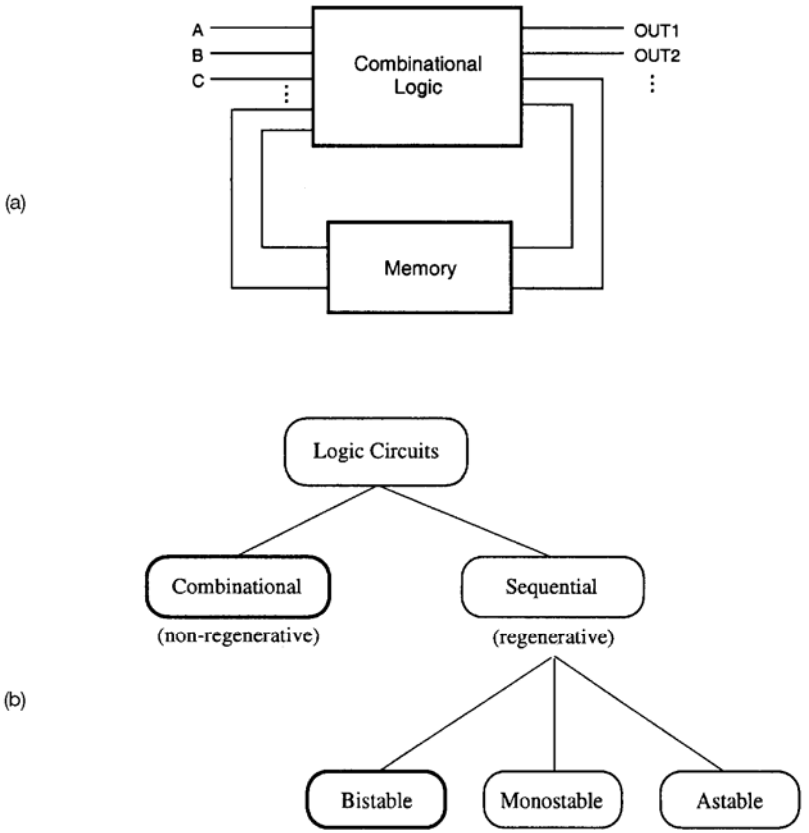


Figure 8.1 (a) Sequential circuit consisting of a combinational logic block and a memory block in the feedback loop. (b) Classification of logic circuits based on their temporal behavior.

Behavior of bistable elements

- Two identical cross-coupled inverter circuits
  - $v_{o1}=v_{i2}$, $v_{o2}=v_{i1}$
  - The two voltage transfer characteristics, v_{o1}-v_{i1}, and v_{o2}-v_{i2}
    - Intersecting at three points
    - If the circuit is initially operating at one of these two stable point
      - Preserve this state unless it is forced externally to change its operating point
      - Gain is smaller than unity (at the two operating points)
        - » Need sufficiently large voltage perturbation
    - The third operating point
      - The voltage gains are larger than unity
      - A small perturbation at the input of any of the inverters will be amplified
      - Causing the operating to move to one of the stable operating point

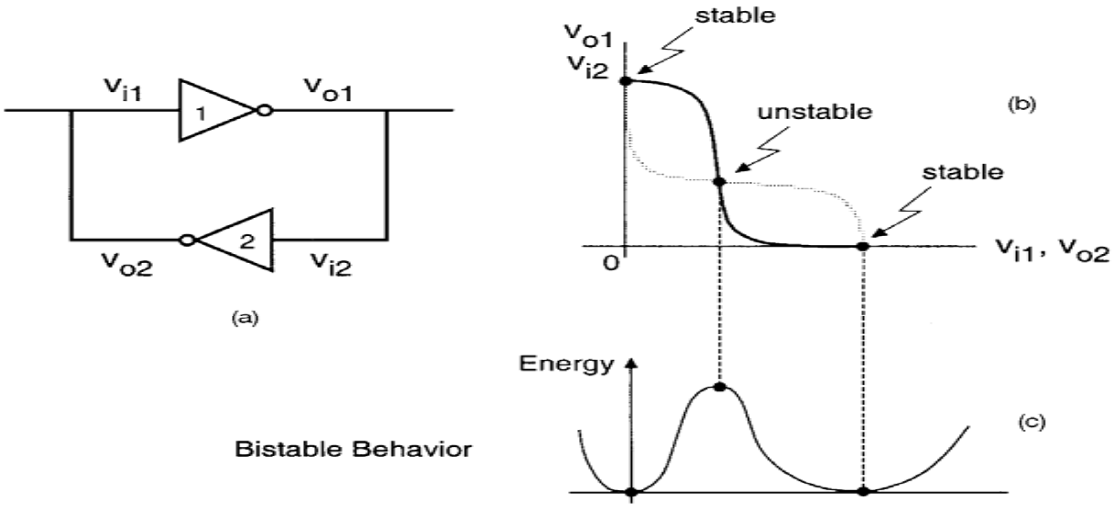


Figure 8.2 Static behavior of the two-inverter basic bistable element: (a) Circuit schematic. (b) Intersecting voltage transfer curves of the two inverters, showing the three possible operating points. (c) Qualitative view of the potential energy levels corresponding to the three operating points.

CMOS two-inverter bistable element

- At the unstable operating point
  - All four the transistor are in saturation
  - Resulting in maximum loop gain for the circuit
  - Small voltage perturbation
    - Output voltage diverse and eventually settle at V_{OH} and V_{OL}

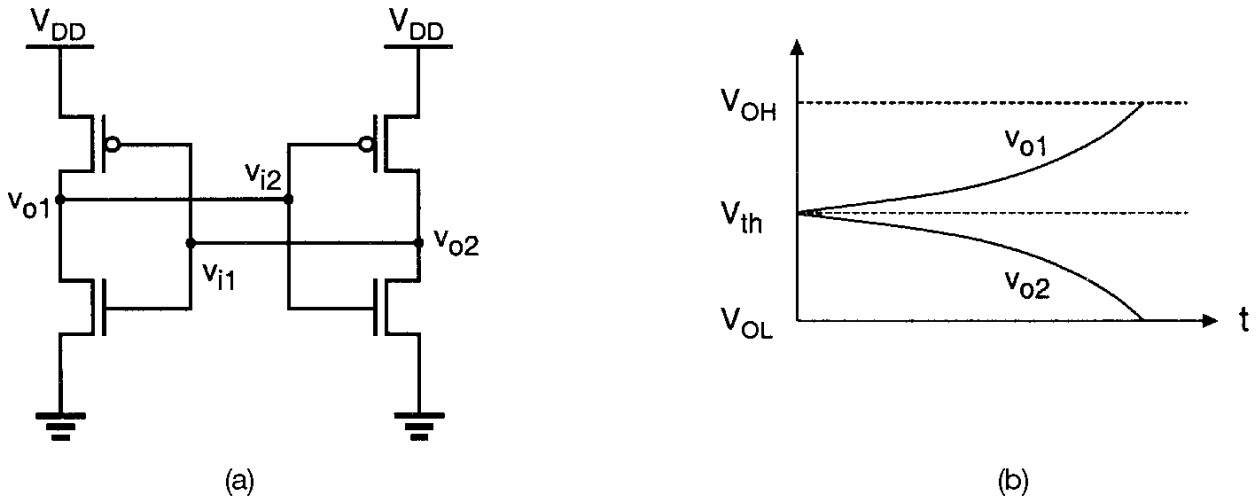


Figure 8.3 (a) Circuit diagram of a CMOS bistable element. (b) One possibility for the expected time-domain behavior of the output voltages, if the circuit is initially set at its unstable operating point.

Small-signal input and output, propagation of a transient

Initially operating at $v_{o1} = v_{o2} = v_{th}$, i.e. at the unstable operating point

Assume $C_g >> C_d$ for each inverter

Small signal drain current, $i_{g1} = i_{d2} = g_m v_{g2}$, $i_{g2} = i_{d1} = g_m v_{g1}$ where $v_{g1} = \frac{q_1}{C_g}$, $v_{g2} = \frac{q_2}{C_g}$, q_1 and q_2 are the gate charg

$$i_{g1} = C_g \frac{dv_{g1}}{dt}, i_{g2} = C_g \frac{dv_{g2}}{dt} \Rightarrow g_m v_{g2} = C_g \frac{dv_{g1}}{dt}, g_m v_{g1} = C_g \frac{dv_{g2}}{dt} \Rightarrow \frac{g_m}{C_g} q_2 = \frac{dq_1}{dt}, \frac{g_m}{C_g} q_1 = \frac{dq_2}{dt}$$

$$\Rightarrow \frac{g_m}{C_g} q_1 = \frac{C_g}{g_m} \frac{d^2 q_1}{dt^2} \Rightarrow \frac{d^2 q_1}{dt^2} = \left(\frac{g_m}{C_g}\right)^2 q_1$$

This equation can also be expressed in a more simplified form by using τ_0, the transit time constant

$$\frac{d^2 q_1}{dt^2} = \frac{1}{\tau_0^2} q_1 \text{ with } \tau_0 = \frac{C_g}{g_m}$$

The time - domain solution for $q_1(t) = \frac{q_1(0) - \tau_0 q_1'(0)}{2} e^{-\frac{t}{\tau_0}} + \frac{q_1(0) - \tau_0 q_1'(0)}{2} e^{+\frac{t}{\tau_0}}$

where the initial condition is $q_1(0) = C_g \cdot v_{g1}(0)$, note that $v_{g1} = v_{o2}$, $v_{g2} = v_{01}$

$$v_{o2}(t) = \frac{1}{2}\left(v_{o2}(0) - \tau_0 v_{02}'(0)\right) e^{-\frac{t}{\tau_0}} + \frac{1}{2}\left(v_{o2}(0) + \tau_0 v_{02}'(0)\right) e^{+\frac{t}{\tau_0}}$$

$$v_{o1}(t) = \frac{1}{2}\left(v_{o1}(0) - \tau_0 v_{01}'(0)\right) e^{-\frac{t}{\tau_0}} + \frac{1}{2}\left(v_{o1}(0) + \tau_0 v_{01}'(0)\right) e^{+\frac{t}{\tau_0}}$$

$$\Rightarrow v_{o1}(t) \approx \frac{1}{2}\left(v_{o1}(0) + \tau_0 v_{01}'(0)\right) e^{+\frac{t}{\tau_0}}, v_{o2}(t) \approx \frac{1}{2}\left(v_{o2}(0) + \tau_0 v_{02}'(0)\right) e^{+\frac{t}{\tau_0}}$$

Note that the magnitude of both output voltages increases exponentially with time

Depending on the polarity of the initial small perturbations $dv_{o1}(0)$ and $dv_{o2}(0)$,

the output voltages of both inverters will diverge from their initial value of V_{th} to either V_{OL} or V_{OH}

While the bistable circuit is settling from its unstable operating point into one of its stable operating points,

we can envison a signal traveling the loop consisting of the two cascaded inverters several times.

The time - domain behavior of the output voltage v_{o1} during this period is $\frac{v_{o1}(t)}{v_{o1}(0)} = e^{+\frac{t}{\tau_o}}$

If during a time interval T, the signal travels the loop n times, then the equivalent to the same signal propagating along a cascaded inverter chain consisting of $2n$ inverters.

The loop gain $A^n = e^{+\frac{T}{\tau_0}}$

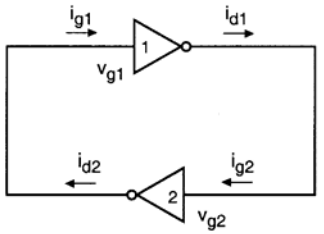


Figure 8.4 Small-signal input and output currents of the inverters.

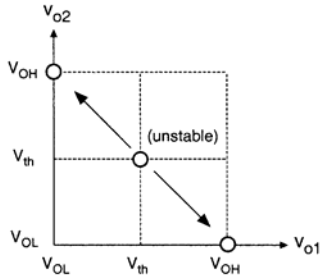
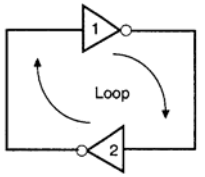


Figure 8.5 Phase-plane representation of the bistable circuit behavior.



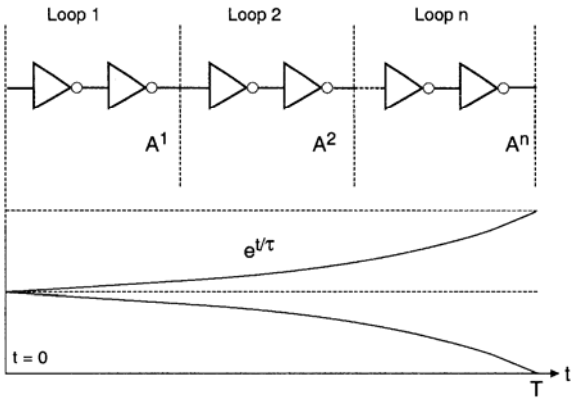


Figure 8.6 Propagation of a transient signal in the two-inverter loop during settling.

SR latch circuit

- The bi-stable element
  - Consisting two cross-coupled inverters has two stable operating states
  - Preserving its state as long as the power supply is provided
    - A simple memory function of holding its state
    - However, no provision for allowing its state to be changed externally from one stable operating mode to another
- CMOS SR latch
  - Having two triggering inputs, S and R
    - Triggering the circuit from one operating point to the other
  - SR flip-flop
    - Two stable states can be switched back and forth
  - Consisting
    - Two CMOS NOR2 gates
      - One input cross-couple to the output of other NOR gate
      - Another input enables triggering of the circuit

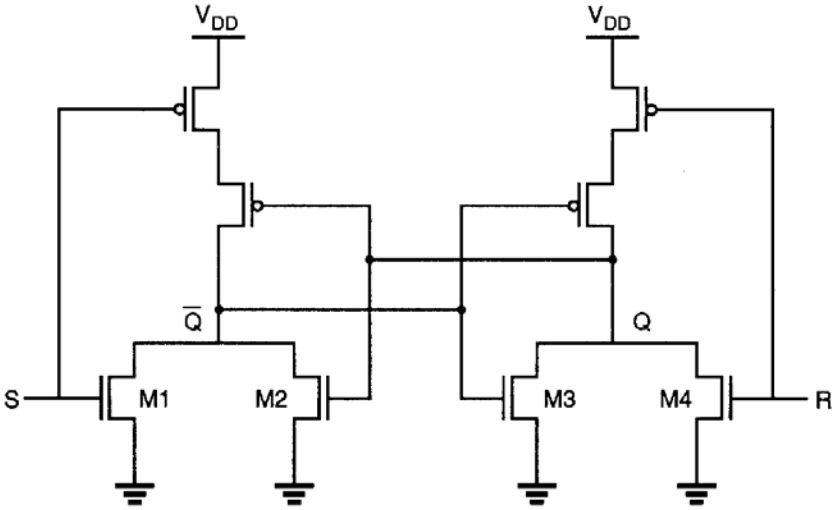


Figure 8.7 CMOS SR latch circuit based on NOR2 gates.

SR latch circuit

- The SR latch has two complementary outputs, Q and –Q
  - Q=1 ⇒ in its “set” state
  - Q=0 ⇒ in its “reset” state
- Gate level schematic
  - Two NOR2 gates
  - If both inputs =“0”
    - Operating like the simple cross-coupled bistable element
    - Holding either one of its two stable operating points (states) as determined by the previous inputs
  - If S=1
    - Forcing the output Q=1
  - If R=1
    - Forcing the output Q=0
  - S=1 and R=1, not allowed

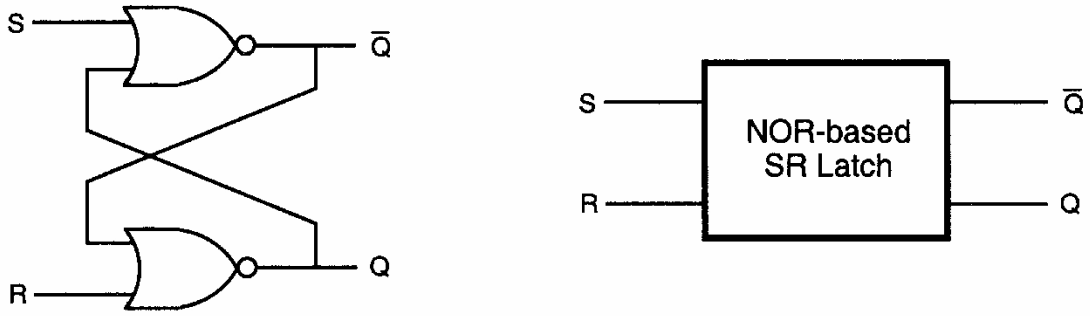


Figure 8.8 Gate-level schematic and block diagram of the NOR-based SR latch.

Table 8.1 Truth table of the NOR-based SR latch circuit

S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
0	0	Q_n	$\overline{Q_n}$	hold
1	0	1	0	set
0	1	0	1	reset
1	1	0	0	not allowed

Operation modes of the transistors in the NOR-based CMOS SR latch circuit

- If $S=V_{OH}$, $R=V_{OL}$
  - M1, M2 on $\Rightarrow$ node $-Q=V_{OL}=0$
  - M3, M4 off $\Rightarrow$ node $Q=V_{OH}$
- If $S=V_{OH}$, $R=V_{OL}$, the situation will reverse
- If $S=V_{OL}$, $R=V_{OL}$, there are two possibilities
  - Depending on the previous state of the SR latch
  - Either M2 or M3 on (while M1, M4 off)
    - Generating a logic low level of $V_{OL}=0$ at one of the output nodes
    - While the complementary output node is at V_{OH}

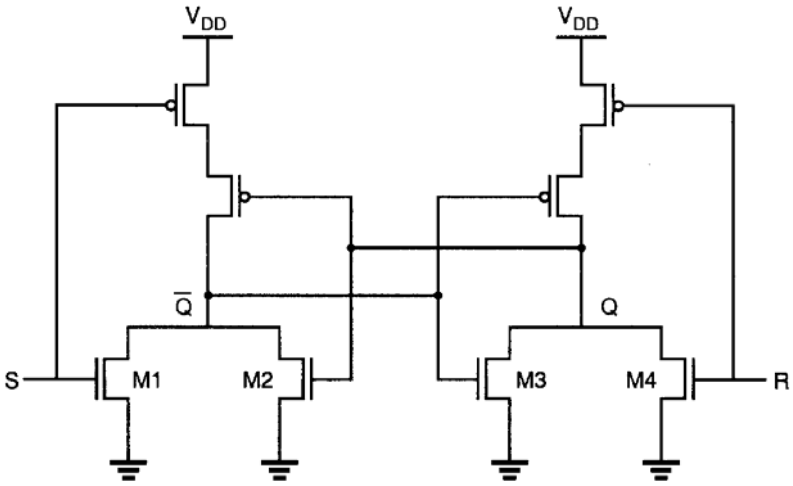


Figure 8.7 CMOS SR latch circuit based on NOR2 gates.

Table 8.2 Operation modes of the transistors in the NOR-based CMOS SR latch circuit

S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
V_{OH}	V_{OL}	V_{OH}	V_{OL}	M1 and M2 on, M3 and M4 off
V_{OL}	V_{OH}	V_{OL}	V_{OH}	M1 and M2 off, M3 and M4 on
V_{OL}	V_{OL}	V_{OH}	V_{OL}	M1 and M4 off, M2 on, or
V_{OL}	V_{OL}	V_{OL}	V_{OH}	M1 and M4 off, M3 on

Transient analysis of the SR latch circuit

$$C_Q = C_{gb,2} + C_{gb,5} + C_{db,3} + C_{db,4} + C_{db,7} + C_{SB,7} + C_{db,8}$$

$$C_{\overline{Q}} = C_{gb,3} + C_{gb,7} + C_{db,1} + C_{db,2} + C_{db,5} + C_{SB,5} + C_{db,6}$$

Assuming that the latch is initially reset and that a set operation is being performed by applying S ="1" and R ="0", the rise time associated with node Q can now be estimated as follows

$$\tau_{\text{rise, Q}}(\text{SR - latch}) = \tau_{\text{rise, Q}}(\text{NOR2}) + \tau_{\text{fall, }\overline{\text{Q}}}(NOR2)$$

The calculation of the switching time $\tau_{\text{rise,Q}}$ requires two separate calculations for the rise and fall times of the NOR2 gates

First, M1 turn on $\Rightarrow \overline{\text{Q}}$ falling from high to low; followed M3 turn off $\Rightarrow$ Q rising from low to high

both M2 and M4 can be assumed to be off in this process

(although M2 can be turned on as Q rises)

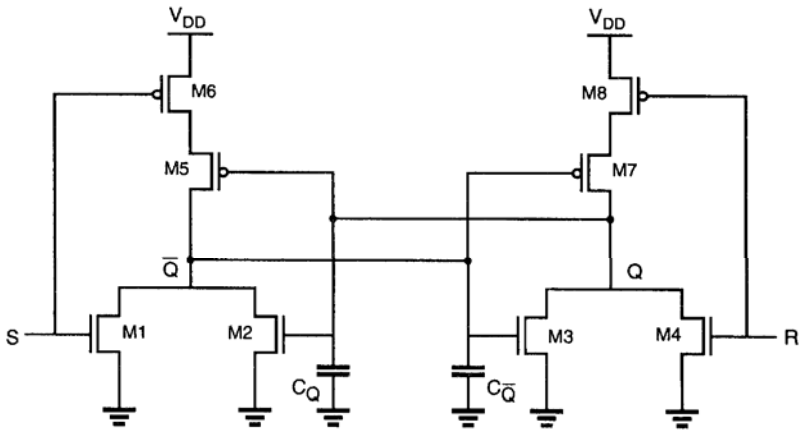


Figure 8.9 Circuit diagram of the CMOS SR latch showing the lumped load capacitances at both output nodes.

Depletion load nMOS SR latch circuit

- The operation principle is identical to that of the CMOS SR latch
  - In terms of power dissipation and noise margins

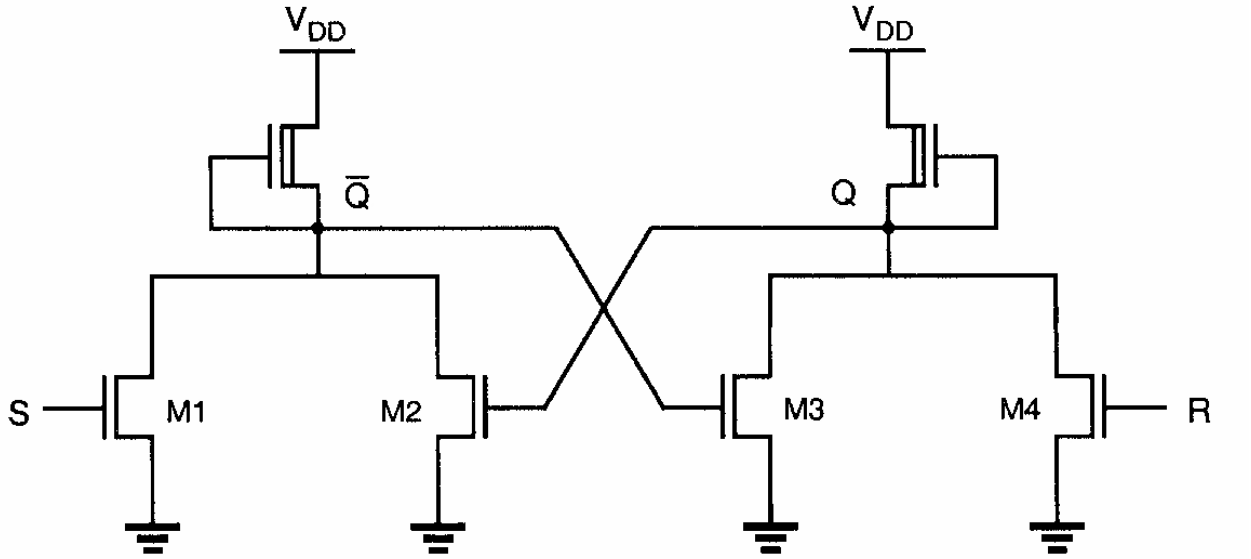


Figure 8.10 Depletion-load nMOS SR latch circuit based on NOR2 gates.

CMOS SR latch circuit based on NAND2 gates

- S=1, R=1⇒ holding state
- S=0, R=1⇒ Q=1, -Q=0 (set the latch)
- S=1, R=0⇒ Q=0, -Q=1 (reset the latch)
- The NAND-based SR latch responds to *active low* input signals
  - The NOR-based SR latch, which responds to *active high* inputs
- S=0, R=0⇒ Q=0, -Q=0 (not allowed)
- Depletion-load NAND2 gates
  - The same operation
  - Poor static power dissipation and noise margins

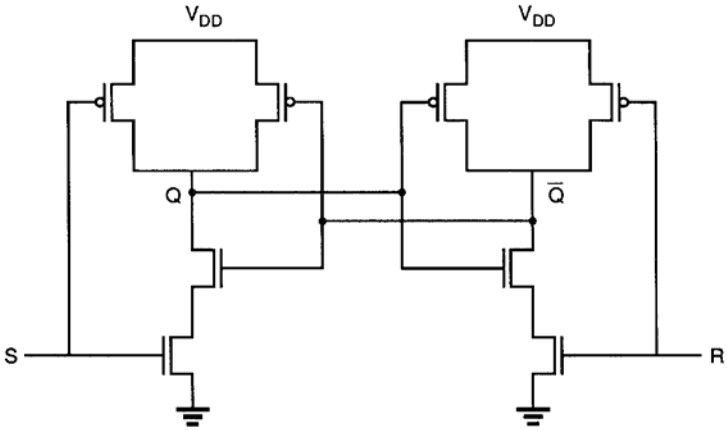


Figure 8.11 CMOS SR latch circuit based on NAND2 gates.

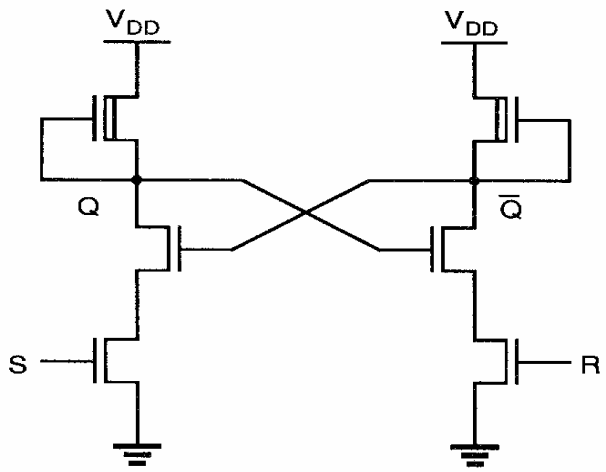
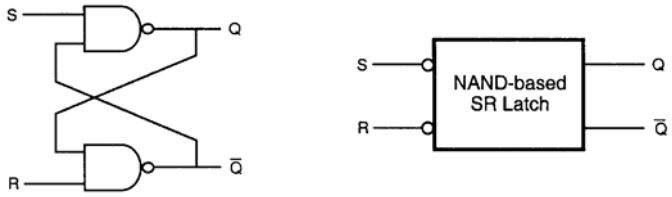


Figure 8.13 Depletion-load nMOS NAND-based SR latch circuit.



S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
0	0	1	1	not allowed
0	1	1	0	set
1	0	0	1	reset
1	1	Q_n	$\overline{Q_n}$	hold

Figure 8.12 Gate-level schematic and block diagram of the NAND-based SR latch.

Clocked SR latch

- Asynchronous sequential circuit
  - Responding to the changes occurring in input signals at a circuit-delay-dependent time point during their operation
- Synchronous operation
  - By adding a gating clock signal to the circuit
  - The outputs will respond to the input levels only during the active period of a clock pulse
- A clocked NOR-based SR latch
  - CK=0
    - The input signal have no influence upon the circuit response
    - Output hold its current state
  - CK=1
    - S and R inputs are permitted to reach the SR latch
  - The circuit is strictly level-sensitive during active clock phases
    - Any changes occurring in the S and R input voltage when the CK level is equal to “1”

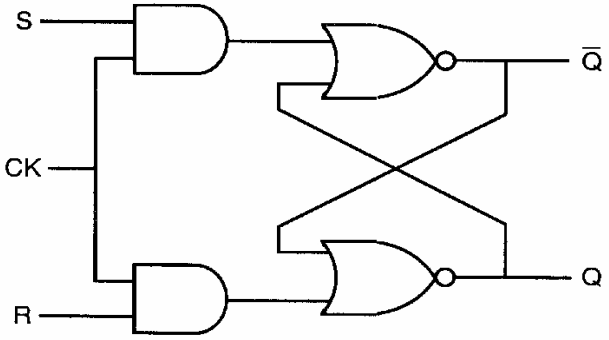


Figure 8.14 Gate-level schematic of the clocked NOR-based SR latch.

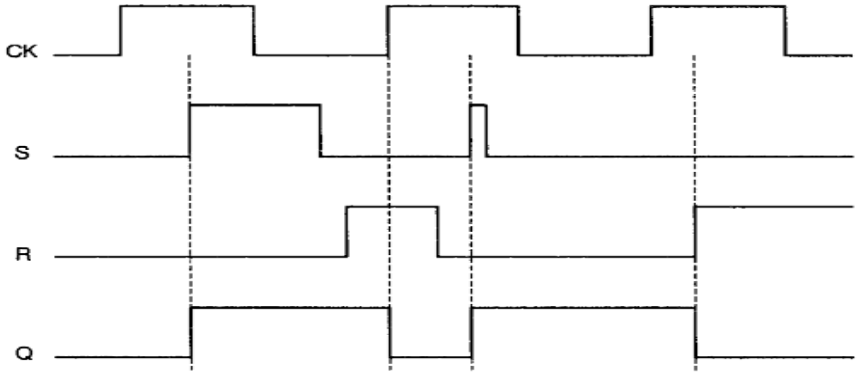


Figure 8.15 Sample input and output waveforms illustrating the operation of the clocked NOR-based SR latch circuit.

AOI based implementation of the clocked NOR-based SR latch

- Very small transistor counts

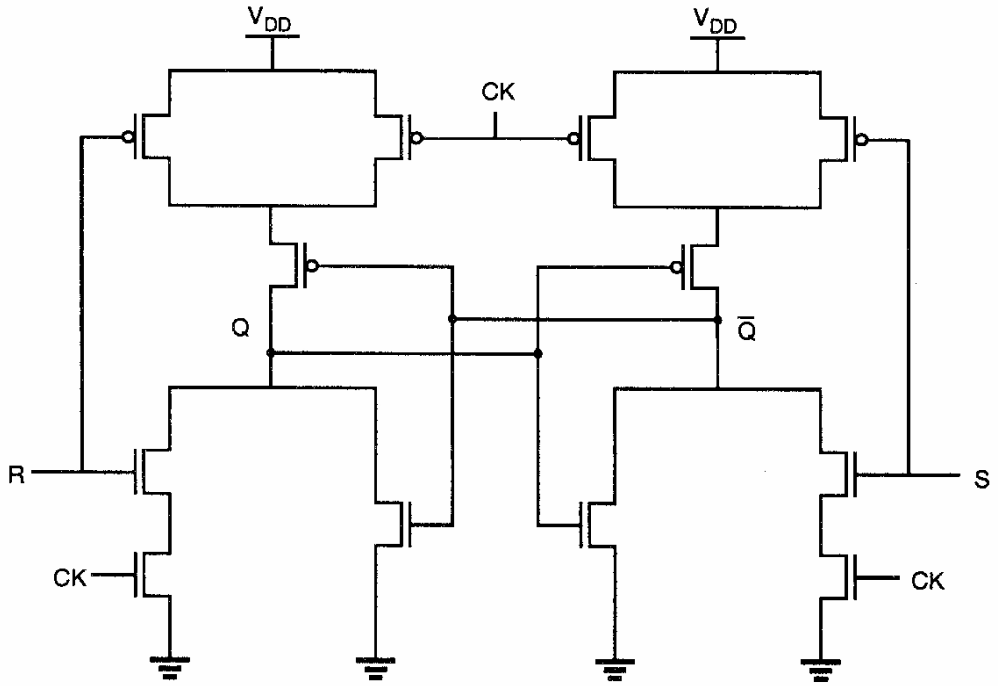


Figure 8.16 AOI-based implementation of the clocked NOR-based SR latch circuit.

Active low

- The changes in the input signal levels will be ignored when the clock is equal to logic “1”
- The input will influence the outputs only when the clock is active, i.e., CK=0

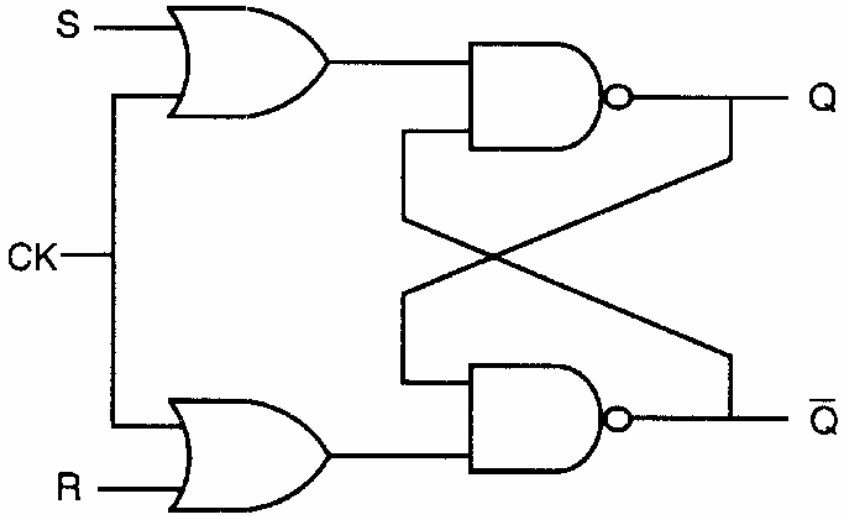


Figure 8.17 Gate-level schematic of the clocked NAND-based SR latch circuit, with active low inputs.

The clocked NAND-based SR latch

- Both the input signals and the CK signal are *active high*
- CK=1
  - S=1, R=0 $\Rightarrow$ Q will be set
  - S=0, R=1 $\Rightarrow$ Q will be reset
- CK=0
  - The latch preserves its state
- Drawback
  - The transistor count is higher than the active low version shown in Fig. 8.17

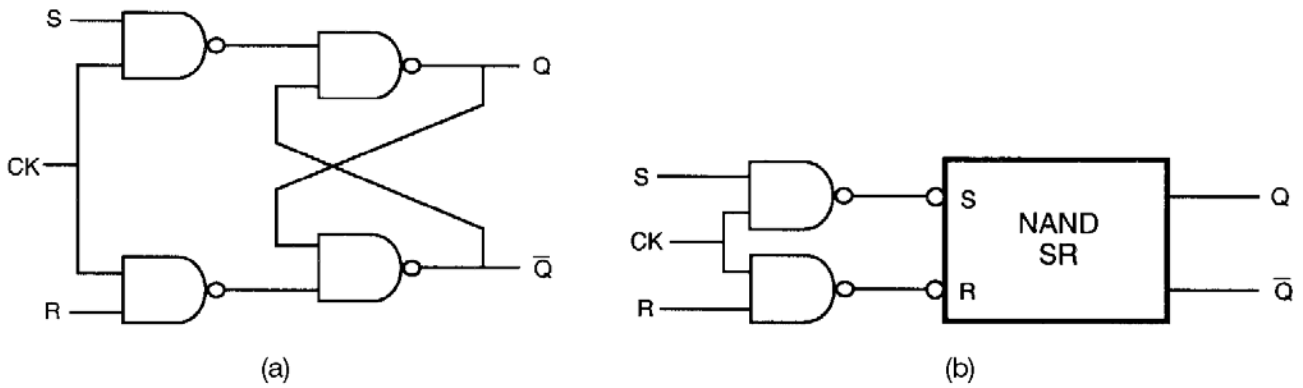


Figure 8.18 (a) Gate-level schematic of the clocked NAND-based SR latch circuit, with active high inputs. (b) Partial block diagram representation of the same circuit.

Clocked JK latch

- All simple and clocked SR latch circuits suffer from the common problem
  - Having a not-allowed input combination
    - Their state becomes indeterminate when both inputs S and R are activated at the same time
- JK latch (JK flip-flop)
  - By adding two feedback lines from the outputs to the inputs (in SR latch)
- NAND-based JK latch
  - Active high inputs

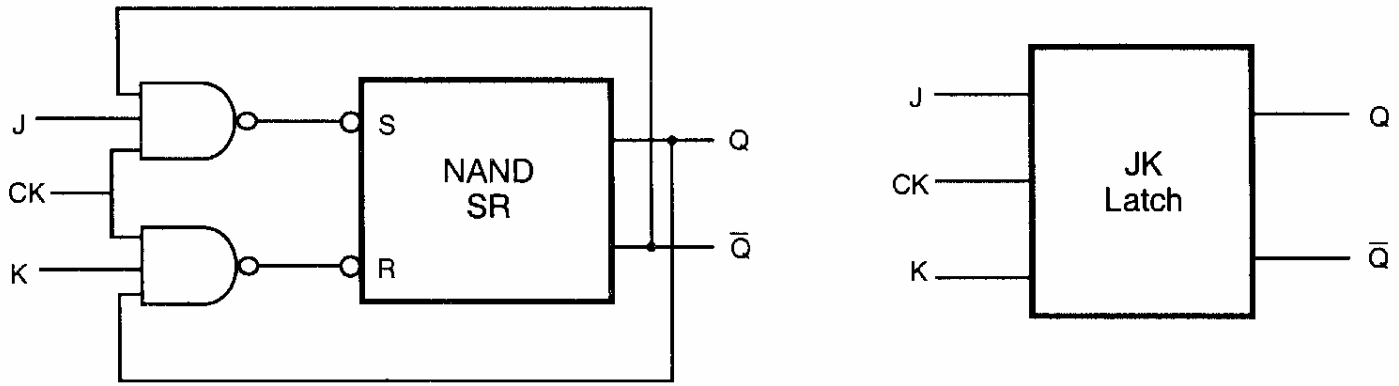


Figure 8.19 Gate-level schematic of the clocked NAND-based JK latch circuit.

All-NAND implementation of the clocked JK latch circuit

- The J and K inputs in this circuit correspond to the set and reset inputs of the basic SR latch
  - J=1, K=0 $\Rightarrow$ set
  - J=0, K=1 $\Rightarrow$ reset
  - J=0, K=0 $\Rightarrow$ preserves its current state
  - J=1, K=1 $\Rightarrow$ the latch simply switches its state due to feedback
    - The JK latch does not have a not-allowed input combination

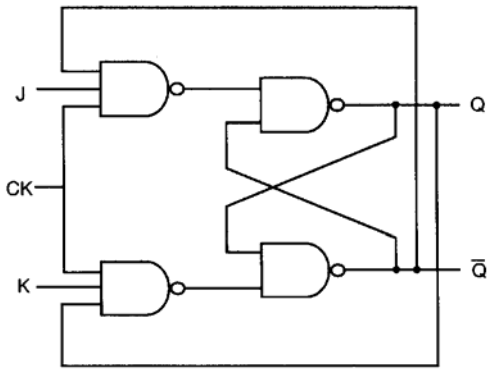


Figure 8.20 All-NAND implementation of the clocked JK latch circuit.

Table 8.3 Detailed truth table of the JK latch circuit

J	K	Q_n	$\overline{Q_n}$	S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
0	0	0	1	1	1	0	1	hold
		1	0	1	1	1	0	
0	1	0	1	1	1	0	1	reset
		1	0	1	0	0	1	
1	0	0	1	0	1	1	0	set
		1	0	1	1	1	0	
1	1	0	1	0	1	1	0	toggle
		1	0	1	0	0	1	

NOR-based implementation of the clocked JK latch

- The AOI-based circuit structure resulted in a relatively low transistor count
- There is no not-allowed input combination for the JK latch
- If J=1, K=1 during the active phase of the clock pulse
  - The output of the circuit will oscillate (toggle) continuously until either the clock becomes inactive (goes to zero), or one of the input signal goes to zero
- To prevent this undesirable timing problem
  - The clock pulse width must be made smaller than the input-to-output propagation delay of the JK latch circuit
  - The clock signal must *go low* before the output level has an opportunity to switch again
  - Assuming that the clock constrain above is satisfied
    - The output of the JK latch will toggle (change its state) only once for each clock pulse, if both inputs are equal to logic "1"
    - Toggle switch

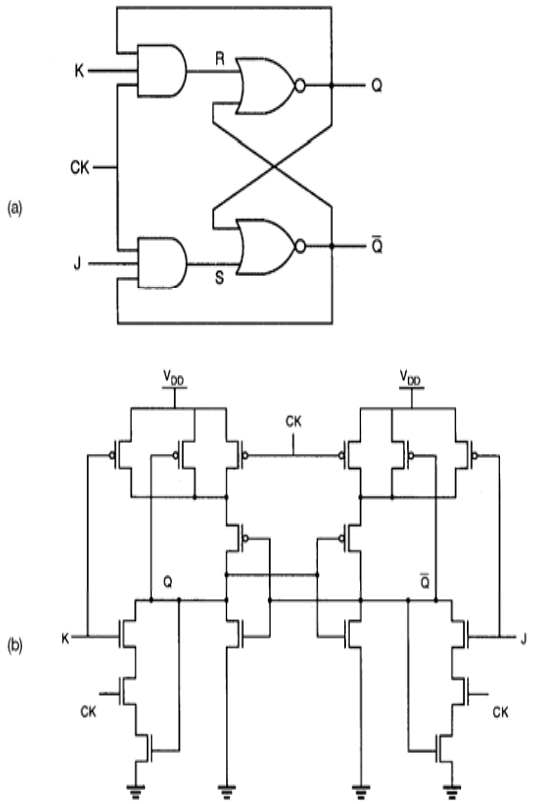


Figure 8.21 (a) Gate-level schematic of the clocked NOR-based JK latch circuit. (b) CMOS AOI realization of the JK latch.

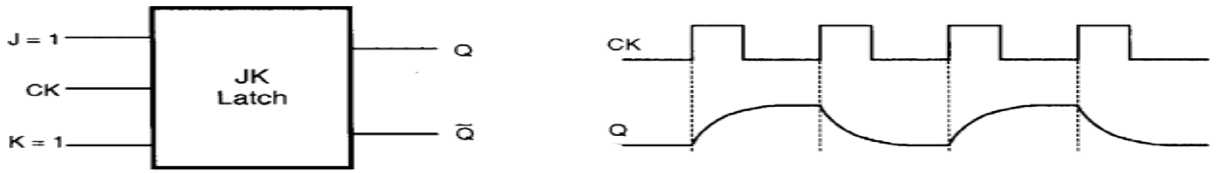


Figure 8.22 Operation of the JK latch as a toggle switch.

Master-slave flip-flop

- The master-slave flip-flop
  - Most of the timing limitations encountered in the previously examined clocked latch circuits can be prevented by using two latch stages in a cascaded configuration
  - The two cascaded stages are activated with opposite clock phases
- Operation
  - Clock high
    - The “master” is activated ⇒ the inputs J and K entered into the flip-flop ⇒ the first stage outputs are set according to the primarily inputs
  - Clock goes to zero
    - The “master” inactive, the “slave” active
    - The output levels of the flip-flop circuit are determined during this second phase

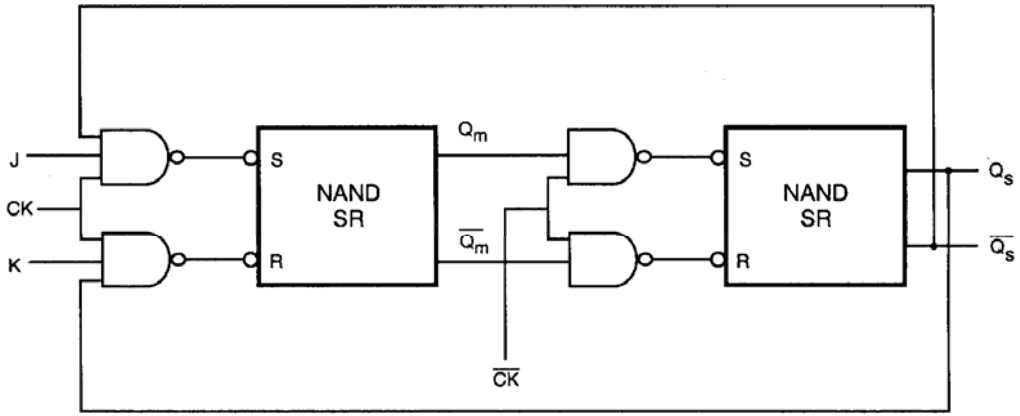


Figure 8.23 Master-slave flip-flop consisting of NAND-based JK latches.

Master-slave flip-flop

- The circuit is never *transparent*
  - A change occurring in the primarily inputs is never reflected directly to the outputs
- Because the master and the slave stages are decoupled from each other, the circuits allows for toggling when J=K=1
- But it eliminates the possibility of the uncontrolled oscillations since only one stage is active at any given time

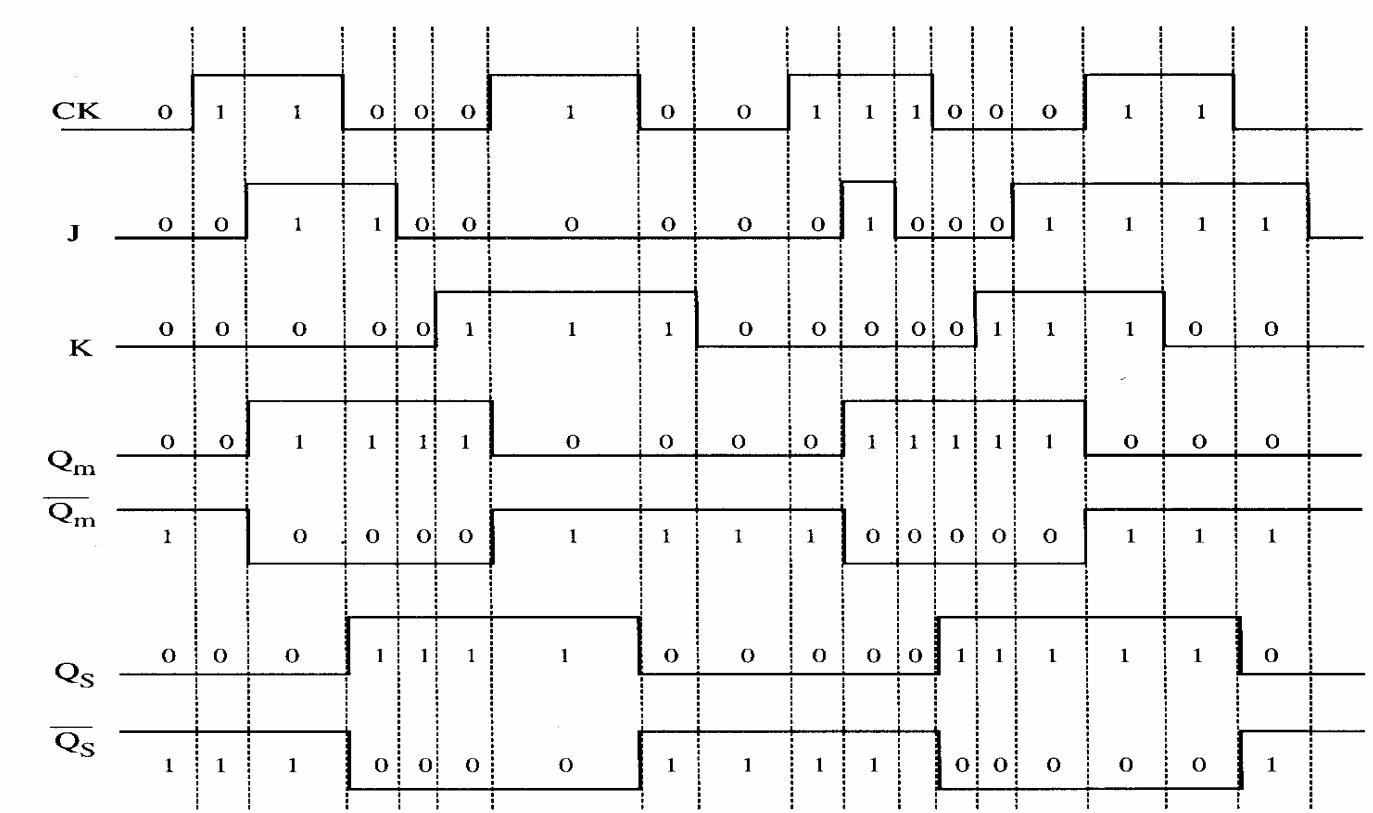


Figure 8.24 Sample input and output waveforms of the master-slave flip-flop circuit.

CMOS D-latch and edge-triggered flip-flop

- Direct CMOS implementations of conventional circuits such as the clocked JK latch or the JK master-slave flip-flop tend to require a large number of transistors
- The simple D-latch circuit
  - Simpler, fewer transistors
  - Operation:
    - When the clock is active $\Rightarrow$ the output Q=the input D
    - When the clock goes to zero $\Rightarrow$ the output will preserve its state
    - The CK input acts as an enable signal which allows data to be accepted into the D-latch
  - Application
    - Temporary storage of data or as a delay element

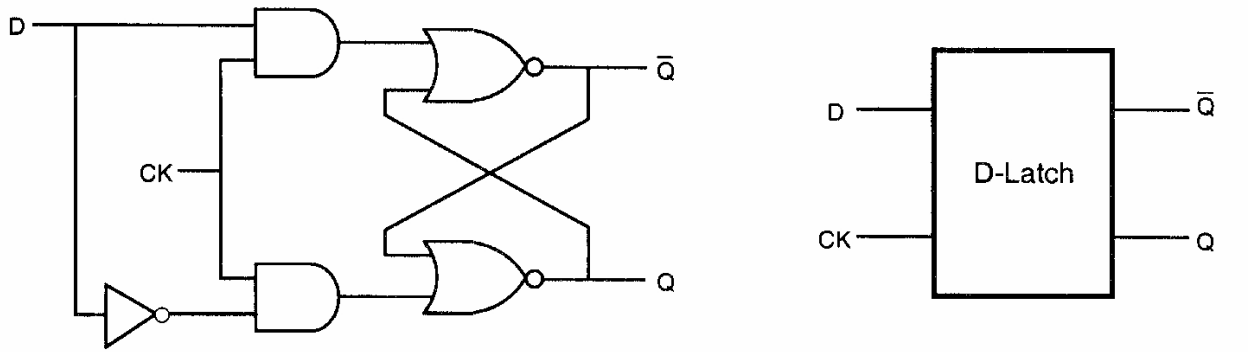


Figure 8.26 Gate-level schematic and the block diagram view of the D-latch.

CMOS implementation of the D-latch

- Circuit diagram
  - Two-inverter loop and two CMOS transmission gate (TG) switches
- Operation
  - CK high $\Rightarrow$ the input signal is accepted (latched) into the circuit
  - CK low $\Rightarrow$ this information is preserved as the state of the inverter loop
  - Timing diagram
    - The valid D input must be stable for a short time before (setup time, t_{setup}) and after (hold time, t_{hold}) the negative clock transition, during which the input switch opens and the loop switch closes
    - Once the inverter loop is completed by closing the loop switch, the output will preserve its valid level

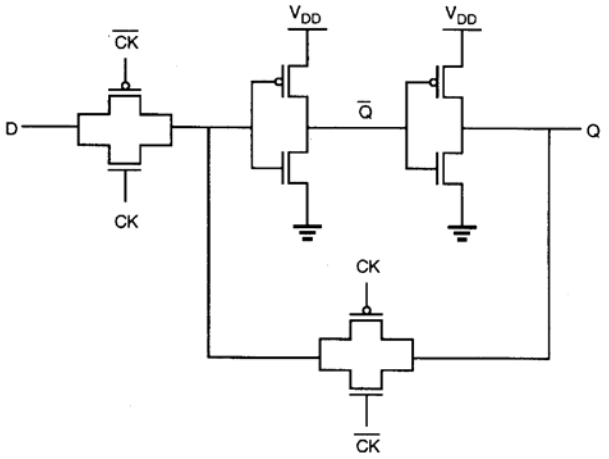


Figure 8.27 CMOS implementation of the D-latch (version 1).

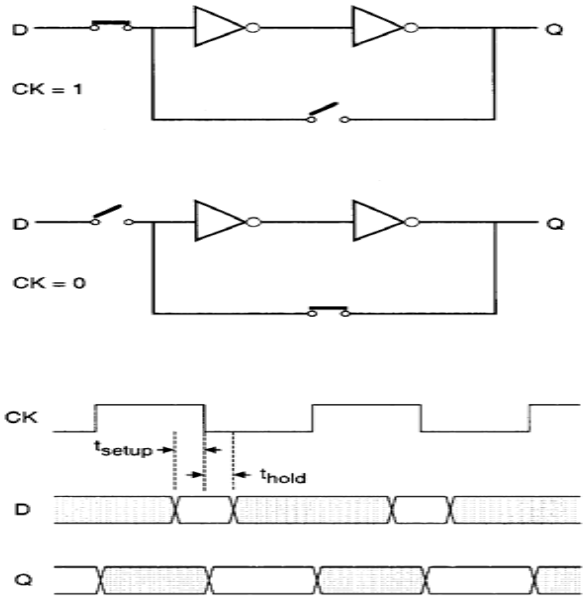


Figure 8.28 Simplified schematic view and the corresponding timing diagram of the CMOS D-latch circuit, showing the setup time and the hold time.

CMOS implementation of the D-latch (version 2)

- Circuit consisting
  - Two tri-state inverters, driven by the clock signal and its inverse
- Operation
  - CK high
    - The first tri-state inverter accepts the input signal
    - The second tri-state inverter is at its high-impedance state
    - The output Q is following the input signal
  - CK low
    - The input buffer becomes inactive
    - The second tri-state inverter completes the two-inverter loop
      - Preserving its state until the next clock pulse

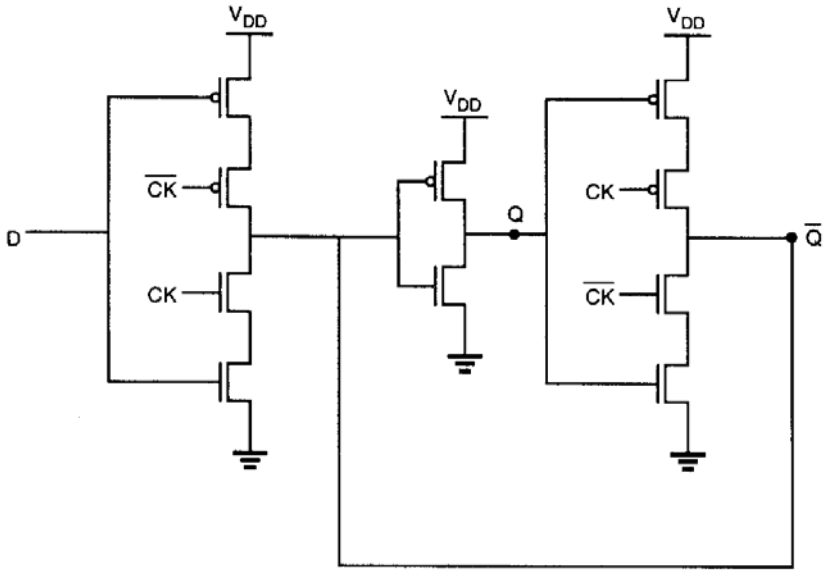


Figure 8.29 CMOS implementation of the D-latch (version 2).

CMOS negative edge-triggered master-slave D flip-flop

- Circuit
  - Cascading two D-latch circuits
  - The first stage (master) is driven by the clock signal
    - Positive level-sensitive
  - The second stage (slave) is driven by the inverted clock signal
    - Negative level-sensitive
- Operation
  - CK high
    - Master ⇒ follows D input
    - Slave ⇒ holds the previous value
  - CK: high → low
    - Master ⇒ cease to sample the input and stores the D value at the time of the clock transition
    - Slave ⇒ becomes transparent , Q_s=Q_m
    - The input cannot affect the output because the master stage is disconnected from the D input
  - CK: low → high
    - Salve ⇒ locks in the master latch output
    - Master ⇒ sampling the input against
  - This circuit is a negative edge-triggered D flip-flop by virtue of the fact that it samples the input at the falling edge of the clock pulse

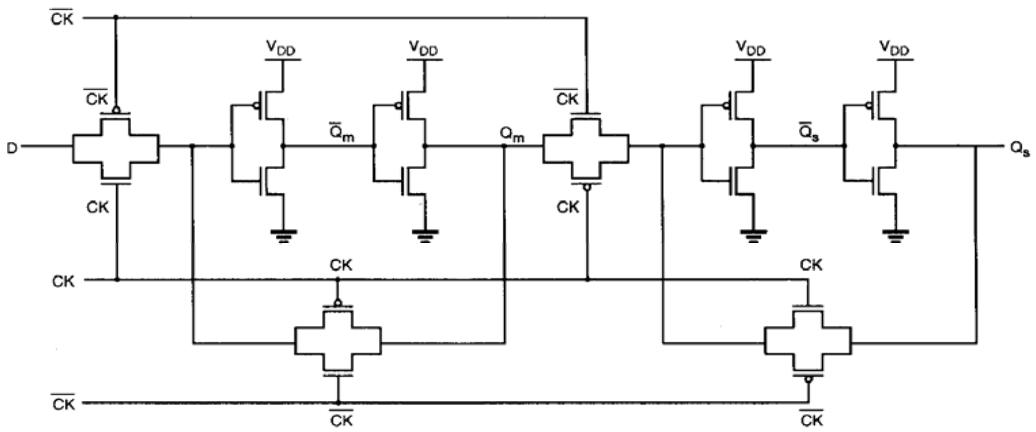


Figure 8.30 CMOS negative (falling) edge-triggered master-slave D flip-flop (DFF).

Simulated input and output waveforms of CMOS DFF

- The output of the master stage latches the applied input (D) when the clock signal is “1”
- The output of the slave stage becomes valid when the clock signal drops to “0”
- The DFF samples the input at every falling edge of the clock pulse

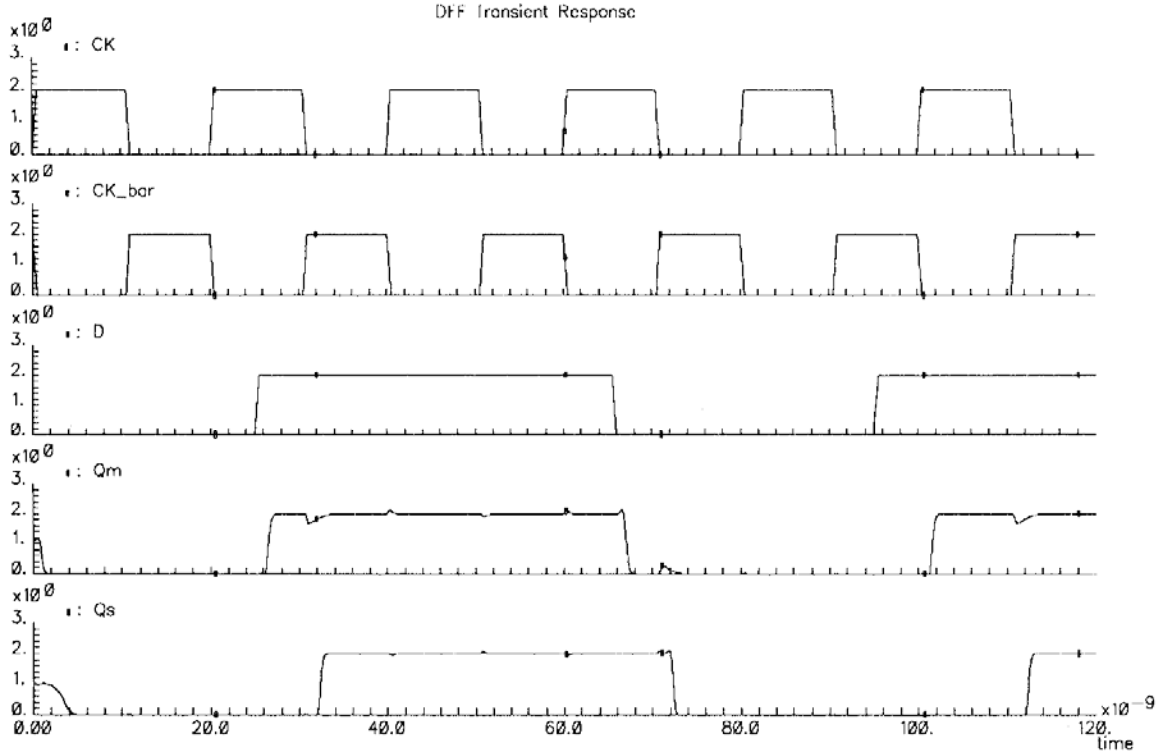


Figure 8.31 Simulated input and output waveforms of the CMOS DFF circuit in Fig. 8.30.

Set-up time violation

- The operation of the DFF circuit can be seriously affected if the master stage experiences a set-up time violation
- If the input D switches from “0” to “1” immediately before the clock transition occurs
  - Master ⇒ fail to latch the correct value
  - Slave ⇒ produces an erroneous output

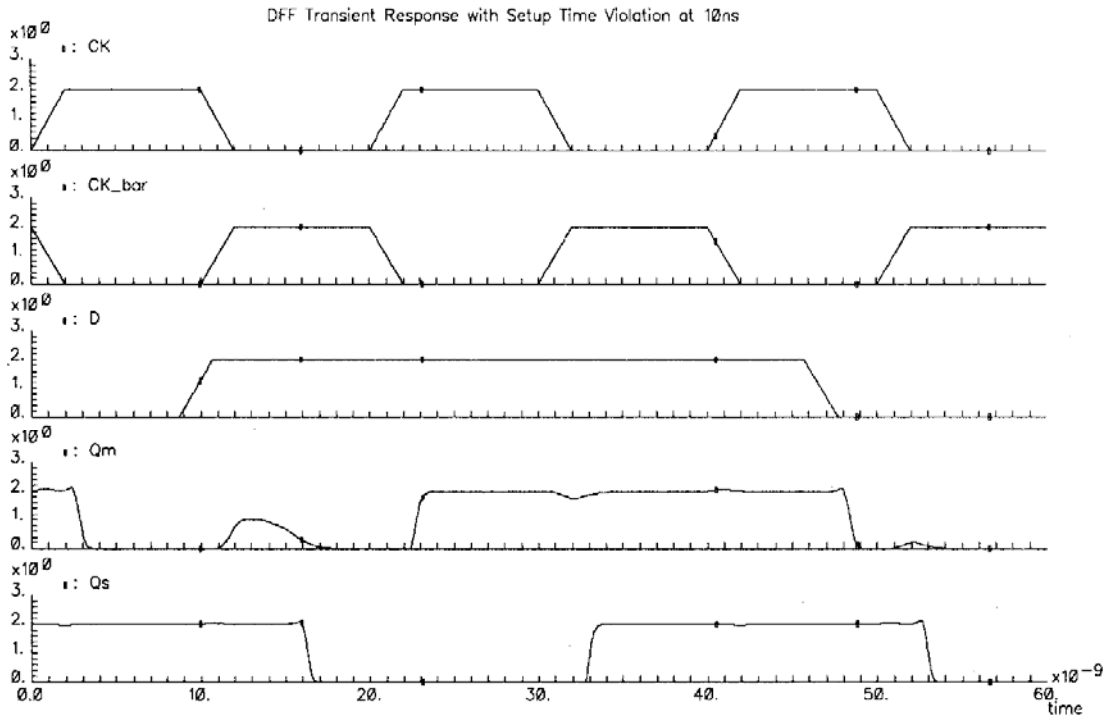


Figure 8.32 Simulated waveforms of the CMOS DFF circuit, showing a set-up time violation for the master stage input at 10 ns. The output of the master stage fails to settle at the correct level.

Layout of DFF

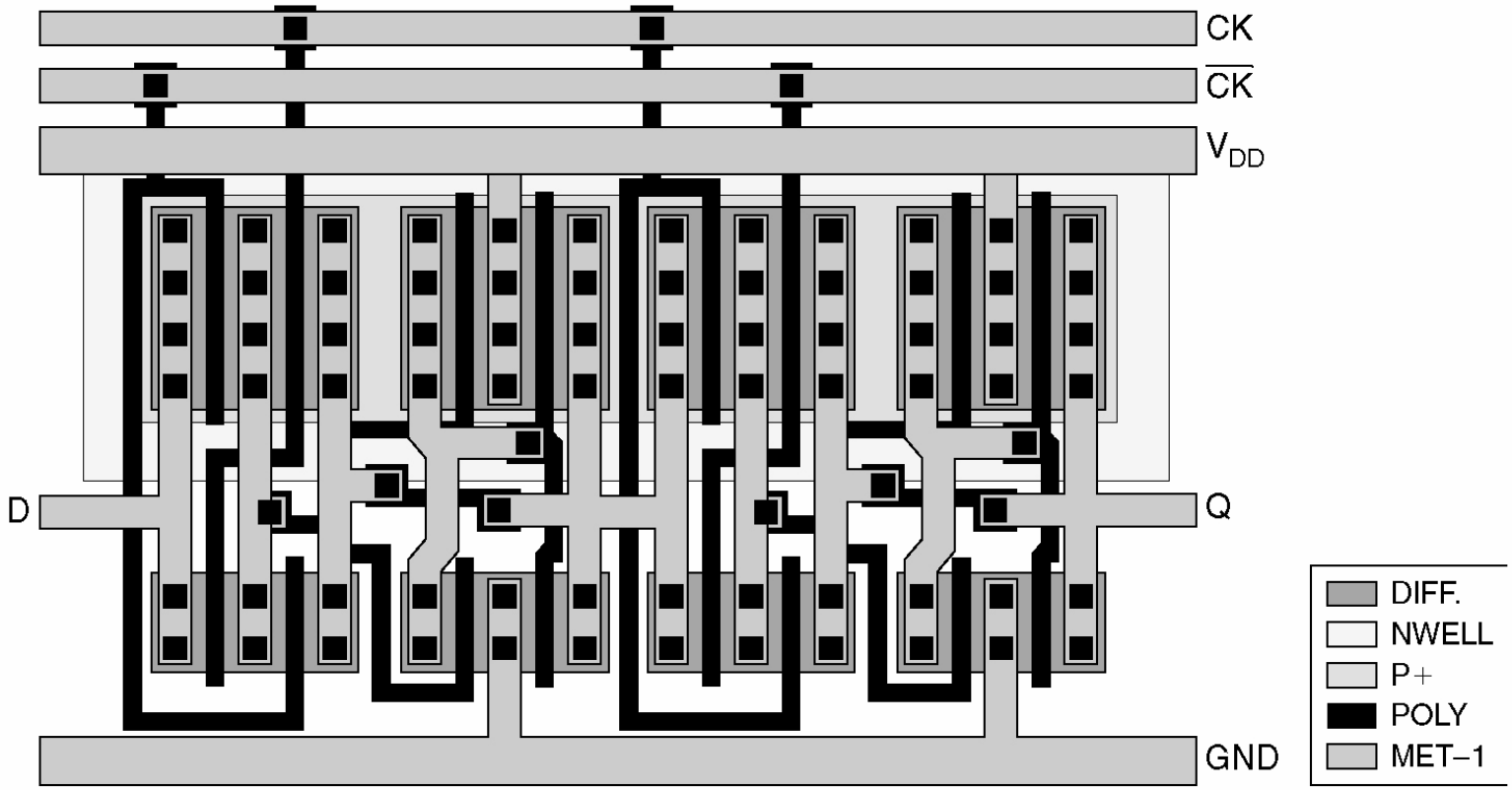


Figure 8.33 Layout of the CMOS DFF shown in Fig. 8.30.

NAND3-based positive edge-triggered DFF

- Initially (S, R, CK, D)=(1, 0, 0, 0) and Q=0
- Second phase (S, R, CK, D)=(1, 0, 1, 1) and Q=0
- Third phase (S, R, CK, D)=(1, 1, 1, 1)
  - The output of gate 2 switches to 0, which in turn sets the output of the last stage SR latch to 1
  - The output of DFF switches to 1 at the positive-going edge of the clock signal, CK

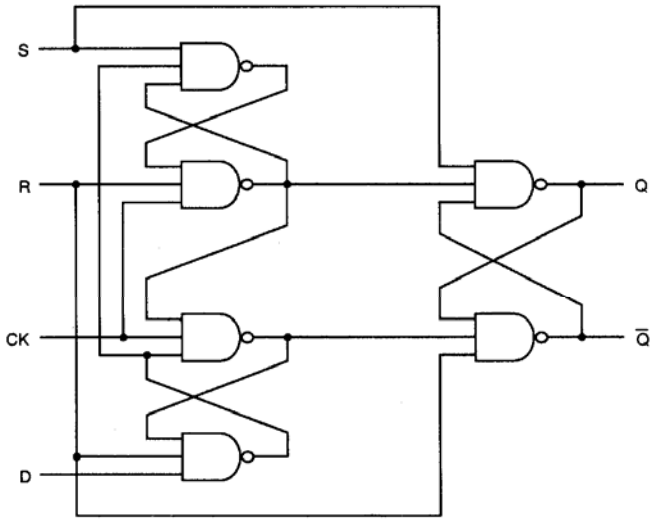


Figure 8.34 NAND3-based positive edge-triggered D flip-flop circuit.

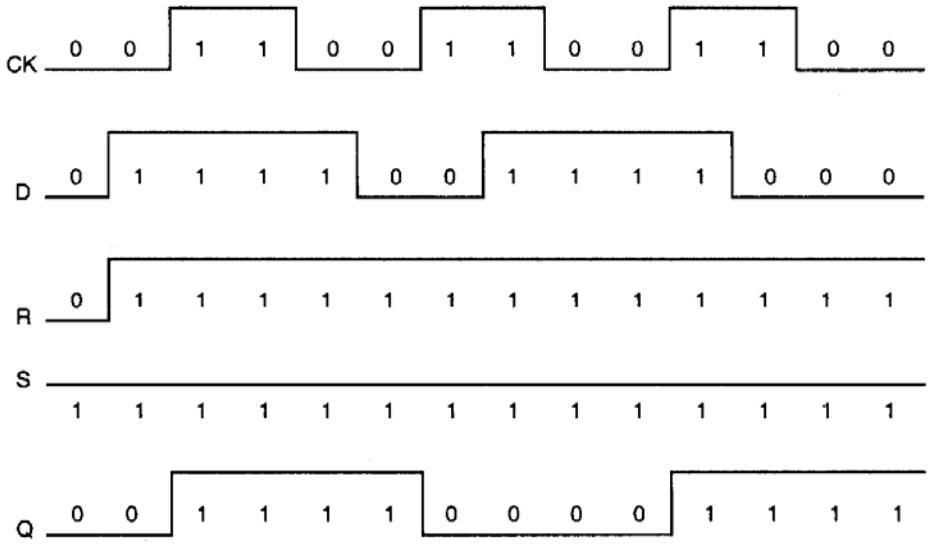


Figure 8.35 Timing diagram of the positive edge-triggered D flip-flop.

Schmitt trigger circuit

- A very useful regenerative circuit
- The schmitt trigger
  - Has an inverter-like voltage transfer characteristic
  - With two different logic threshold voltages
    - For increasing input signal
    - For decreasing input signal
  - Being utilized for the detection of low-to-high and high-to-low switching events in noisy environments

Schmitt trigger circuit- operation (1)

i) At $V_{in} = 0V$

M1 and M2 are turn on $\Rightarrow V_x = V_y = V_{DD} = 5V$

M4 and M5 off, M3 off, M6 on saturation region

$\Rightarrow V_z = V_{DD} - V_{T,6} = 3.5V$

ii) At $V_{in} = V_{T0,n} = 1.0V$

M5 starts to turn on, M4 is still off $\Rightarrow V_x = 5V$

iii) At $V_{in} = 2.0V$

Assume M4 is off, while both M5 and M6 saturation

$$\frac{1}{2}k'\left(\frac{W}{L}\right)_5\left(V_{in} - V_{T0,5}\right)^2 = \frac{1}{2}k'\left(\frac{W}{L}\right)_6\left(V_{DD} - V_z - V_{T0,6}\right)^2$$

$\Rightarrow V_z = 2.976 \Rightarrow V_{GS,4} = 2\text{-}2.976 < V_{T0,n} = 1$, so M4 still off

iv) At $V_{in} = 3.5V$

V_z continues to decrease. Assume M5 linear, M6 saturation

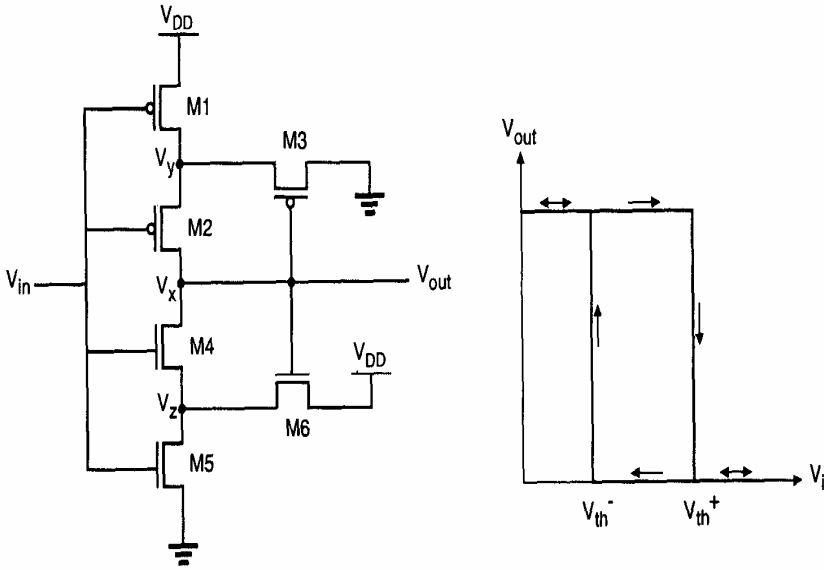
$$\frac{1}{2}k'\left(\frac{W}{L}\right)_5\left[2\left(V_{in} - V_{T0,5}\right)V_z - V_z^2\right] = \frac{1}{2}k'\left(\frac{W}{L}\right)_6\left(V_{DD} - V_z - V_{T0,6}\right)^2$$

$\Rightarrow Vz = 2.2V \Rightarrow V_{GS,4} = 3.5\text{-}2.2 = 1.3 > V_{T0,n} = 1$

At this point, M4 is already on, above assumption no longer valid

V_x is being pulled down toward "0"

We conclude the upper logic threshold voltage $V_{th}^+ \cong 3.5V$




```
CMOS Schmitt Trigger DC analysis
vdd 5 0 dc 5V
vin 1 0 dc 1v
m5 2 1 0 0 mn l=1u w=1u
m4 3 1 2 0 mn l=1u w=2.5u
m6 5 3 2 0 mn l=1u w=3u
m1 4 1 5 5 mp l=1u w=1u
m2 3 1 4 5 mp l=1u w=2.5u
m3 0 3 4 5 mp l=1u w=3u
.model mn nmos vto=1 gamma=0.4 kp=2.5e-5
.model mp pmos vto=-1 gamma=0.4 kp=1.0e-5
.dc vin 0 5 0.1
.print dc v(3)
.end
```

Schmitt trigger circuit- operation (2)

i) At $V_{in} = 5.0V$

M4 and M5 are turn on $\Rightarrow V_x = 0V$

M1 and M2 off, M3 on saturation region

$$\frac{1}{2}k'\left(\frac{W}{L}\right)_3\left(0 - V_y - V_{T,3}\right)^2 = 0 \quad \Rightarrow V_y = 1.5V$$

ii) At $V_{in} = 4.0V$

M1is at the edge of turning on, M2 off, M3 saturation

$\Rightarrow$ the output vol tage is still unchanged

iii) At $V_{in} = 3.0V$

M1 is on and in saturation region, M3 is also saturation

$$\frac{1}{2}k'\left(\frac{W}{L}\right)_1\left(V_{in} - V_{DD} - V_{T0,p}\right)^2 = \frac{1}{2}k'\left(\frac{W}{L}\right)_3\left(0 - V_y - V_{T,3}\right)^2$$

$\Rightarrow V_{in} = 2.02 \Rightarrow V_{GS,2} = 3\text{-}2.02 = 0.98 > V_{T0,p} = -1$

$\Rightarrow$ M2 is still off at this point

iv) At $V_{in} = 1.5V$

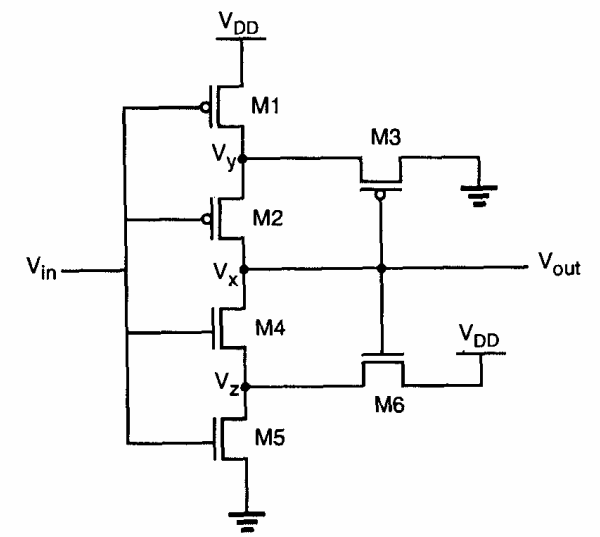
If M2 is still off, M1 linear, M3 saturation

$$\frac{1}{2}k'\left(\frac{W}{L}\right)_1\left[2\left(V_{in} - V_{DD} - V_{T0,p}\right)\left(V_y - V_{DD}\right) - \left(V_y - V_{DD}\right)^2\right] = \frac{1}{2}k'\left(\frac{W}{L}\right)_3\left(0 - V_y - V_{T,3}\right)^2$$

$\Rightarrow V_y = 2.79V$

At this point, M2 is already tu rn on $\Rightarrow$ the output vol tage is being pull up to V_{DD}

We conclude that the lower logic threshold voltage $V_{th}^- \cong 1.5V$



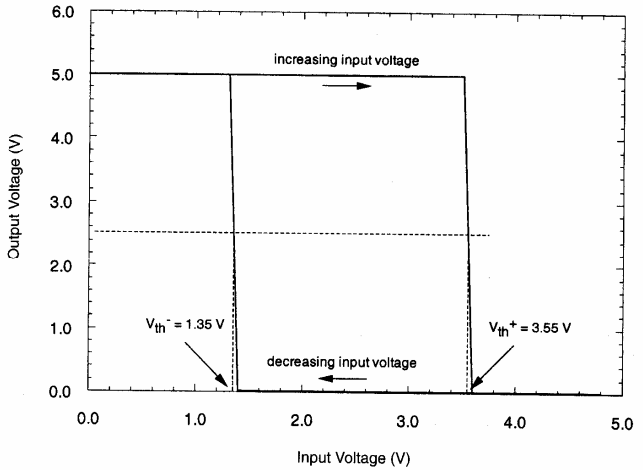


Figure 8.36 Simulated output voltage waveforms of the CMOS Schmitt trigger circuit, for increasing and for decreasing input voltage.