CMOS

Digital Integrated Circuits

Analysis and Design

Chapter 7

Combinational MOS Logic Circuits

Introduction

- Combination logic circuit
  - Performing Boolean operations between input and output
  - Static and dynamic characteristics
- MOS depletion-load gates
  - Emphasize the load concept
  - NAND, NOR
- CMOS logic circuit
- CMOS transmission gates
- Transmission gate (TG) logic circuits
- In most general form
  - A multiple-input, single-output system
  - Using positive logic convention

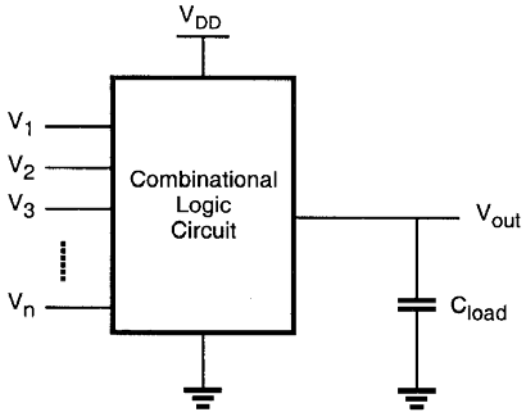
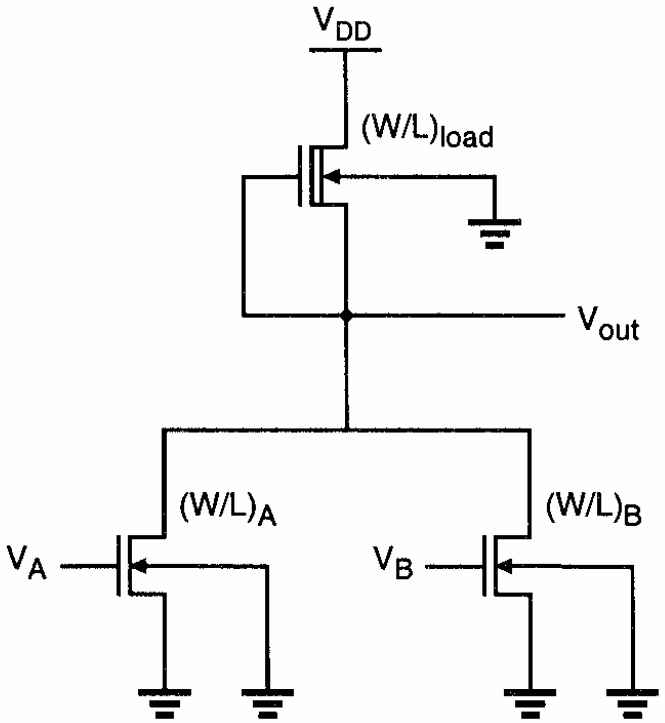


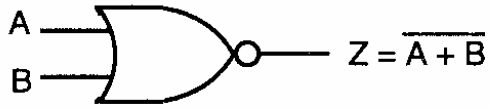
Figure 7.1 Generic combinational logic circuit (gate).

MOS logic circuits with depletion nMOS loads

- Two-input NOR gate
  - Calculation of VOH
  - Calculation of VOL
  - General NOR structure with multiple inputs
  - Transient analysis of NOR gate
- Two-input NAND gate
  - General NAND structure with multiple inputs
  - Transient analysis of NOR gate

Two-input NOR gate





V_A	V_B	V_{out}
low	low	high
low	high	low
high	low	low
high	high	lower

Figure 7.2 A two-input depletion-load NOR gate, its logic symbol, and the corresponding truth table. Note that the substrates of all transistors are connected to ground.

Calculation of V_{OH}, V_{OL}

Calculation of V_{OH}

When V_A and V_B are lower than threshold voltage $\Rightarrow$ both off

$$I_{D,load} = \frac{k_{n,load}}{2} \cdot \left[2\left|V_{T,load}\left(V_{OH}\right)\right| \cdot \left(V_{DD} - V_{OH}\right) - \left(V_{DD} - V_{OH}\right)^2 \right] = 0 \text{ than } V_{OH} = V_{DD}$$

Calculation of V_{OL}

Three case : (i)$V_A = V_{OH}$ $V_B = V_{OL}$ (ii)$V_A = V_{OL}$ $V_B = V_{OH}$ (iii)$V_A = V_{OH}$ $V_B = V_{OH}$

For the first two case : in case (i) $k_R = \dfrac{k_{driver,A}}{k_{load}} = \dfrac{k'_{n,driver}\left(\dfrac{W}{L}\right)_A}{k'_{n,load}\left(\dfrac{W}{L}\right)_{load}}$ in case (ii) $k_R = \dfrac{k_{driver,B}}{k_{load}} = \dfrac{k'_{n,driver}\left(\dfrac{W}{L}\right)_B}{k'_{n,load}\left(\dfrac{W}{L}\right)_{load}}$

$$V_{OL} = V_{OH} - V_{T0} - \sqrt{\left(V_{OH} - V_{T0}\right)^2 - \left(\frac{k_{load}}{k_{driver}}\right) \cdot \left|V_{T,load}\left(V_{OL}\right)\right|^2} \quad (7.4)$$

If the (W/L) ratios of both drivers are identical, the two V_{OL} will identical. In case (iii) both transistors are turned on, the saturated load current is the sum of the two linear - mode driver currents

$$I_{D,load} = I_{D,driverA} + I_{D,driverB} \Rightarrow \frac{k_{load}}{2}\left|V_{T,load}\left(V_{OL}\right)\right|2 = \frac{k_{driver,A}}{2}\left[2\left(V_A - V_{T0}\right)V_{OL} - V_{OL}^2\right] + \frac{k_{driver,B}}{2}\left[2\left(V_B - V_{T0}\right)V_{OL} - V_{OL}^2\right]$$

Since the gate voltages of both driver transistors are equal, we can devise an equivalent driver - to - load ratio for the NOR structure

$$k_R = \frac{k_{driver,A} + k_{driver,B}}{k_{load}} = \frac{k'_{n,driver}\left[\left(\dfrac{W}{L}\right)_A + \left(\dfrac{W}{L}\right)_B\right]}{k'_{n,load}\left(\dfrac{W}{L}\right)_{load}} \quad V_{OL} = V_{OH} - V_{T0} - \sqrt{\left(V_{OH} - V_{T0}\right)^2 - \left(\frac{k_{load}}{k_{driver,A} + k_{driver,B}}\right) \cdot \left|V_{T,load}\left(V_{OL}\right)\right|^2} \quad (7.8)$$

The V_{OL} given by (7.8) is lower than the V_{OL} by (7.4)

We usually set $k_{driver,A} = k_{driver,B} = k_R k_{load}$

Generalized NOR structure with multiple inputs

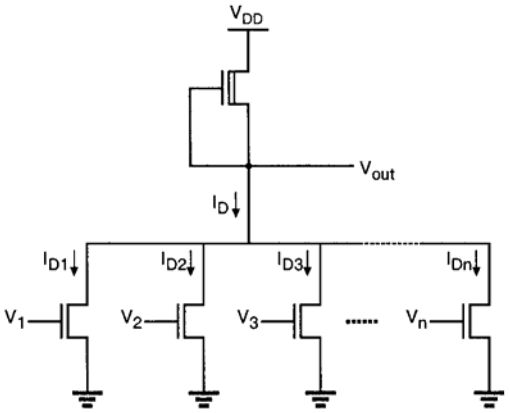


Figure 7.3 Generalized *n*-input NOR gate.

$$I_D = \sum_{k(on)} I_{D,k} = \begin{cases} \sum_{k(on)} \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_k \left[2(V_{GS,k} - V_{T0})V_{out} - V_{out}^2\right] & \textit{linear} \\ \sum_{k(on)} \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_k (V_{GS,k} - V_{T0})^2 & \textit{saturation} \end{cases}$$

$$V_{GS,k} = V_{GS} \qquad \textit{for} \qquad k = 1,2,\ldots,n$$

$$I_D = \begin{cases} \frac{\mu nCox}{2}\left(\sum_{k(on)}\left(\frac{W}{L}\right)_k\right)\left[2(V_{GS} - V_{T0})V_{out} - V_{out}^2\right] & \textit{linear} \\ \frac{\mu nCox}{2}\left(\sum_{k(on)}\left(\frac{W}{L}\right)_k\right)(V_{GS} - V_{T0})^2 & \textit{saturation} \end{cases}$$

$$\left(\frac{W}{L}\right)_{equivalent} = \sum_{k(on)}\left(\frac{W}{L}\right)_k$$

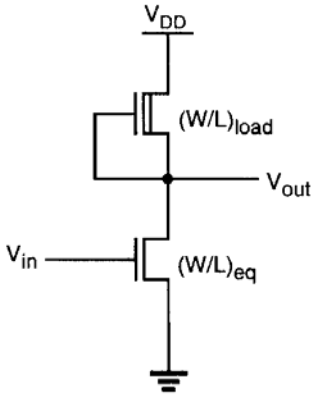


Figure 7.4 Equivalent inverter circuit corresponding to the *n*-input NOR gate.

The driver: no substrate bias effect

The load: suffered substrate biased effect, $V_{SB}=V_{out}$

Transient analysis of NOR gate

- The output load capacitance
  - Being valid for simultaneous as well as for single-input switching
  - The load capacitance C_{load} will be present at the output node even if only one input is active and all other input are low
  - $C_{load} = C_{gd,A} + C_{gd,B} + C_{gd,load} + C_{db,A} + C_{sb,load} + C_{wire}$

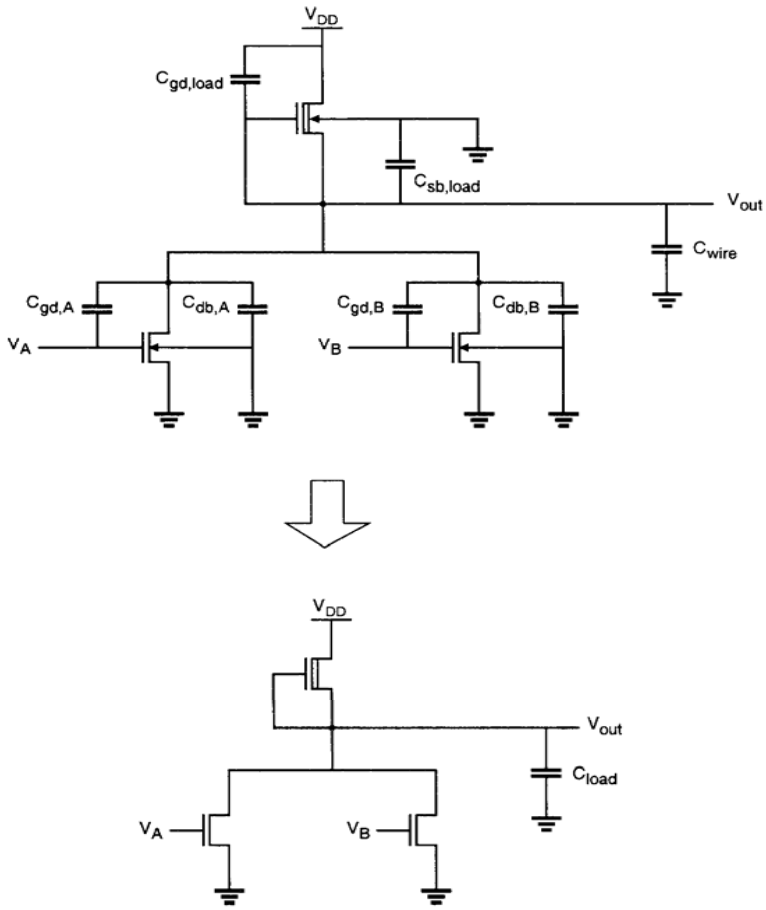
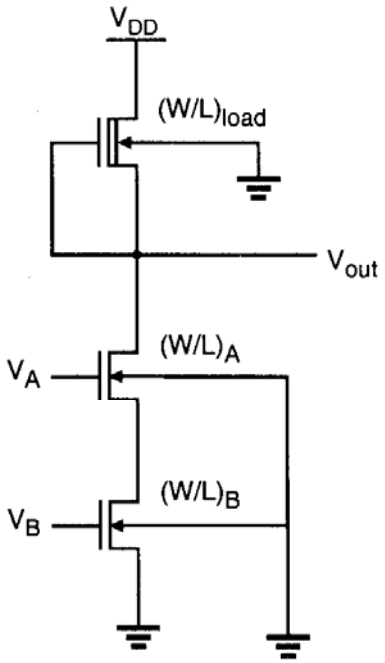
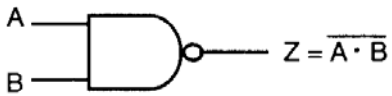


Figure 7.5 Parasitic device capacitances in the NOR2 gate and the lumped equivalent load capacitance. The gate-to-source capacitances of the driver transistors are included in the load of the previous stages driving the inputs A and B.

Two-input NAND gate





V_A	V_B	V_{out}
low	low	high
low	high	high
high	low	high
high	high	low

Figure 7.6 A two-input depletion-load NAND gate, its logic symbol, and the corresponding truth table. Notice the substrate-bias effect for all nMOS transistors except one.

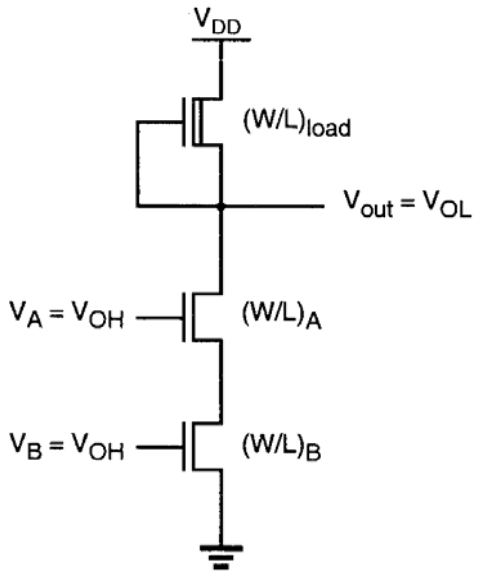


Figure 7.7 The NAND2 gate with both of its inputs at logic-high level.

Calculation of V_{OH}, V_{OL}

When both input equal to $V_{OH} \Rightarrow I_{D,load} = I_{D,driverA} = I_{D,driverB}$

$$\frac{k_{load}}{2}\left|V_{T,load}(V_{OL})\right|^2 = \frac{k_{driver,A}}{2}\left[2(V_{GS,A}-V_{T,A})V_{DS,A}-V_{DS,A}^2\right] = \frac{k_{driver,B}}{2}\left[2(V_{GS,B}-V_{T,B})V_{DS,B}-V_{DS,B}^2\right]$$

Assume $V_{T,A} = V_{T,B} = V_{T0}$

$$V_{DS,A} = V_{OH} - V_{T0} - \sqrt{(V_{OH}-V_{T0})^2 - \left(\frac{k_{load}}{k_{driver,A}}\right)\cdot\left|V_{T,load}(V_{OL})\right|^2}$$

$$V_{DS,B} = V_{OH} - V_{T0} - \sqrt{(V_{OH}-V_{T0})^2 - \left(\frac{k_{load}}{k_{driver,B}}\right)\cdot\left|V_{T,load}(V_{OL})\right|^2}$$

$$V_{OL} \approx 2\left(V_{OH} - V_{T0} - \sqrt{(V_{OH}-V_{T0})^2 - \left(\frac{k_{load}}{k_{driver}}\right)\cdot\left|V_{T,load}(V_{OL})\right|^2}\right)$$

$$I_{D,A} = \frac{k_{driver}}{2}\left[2(V_{GS,A}-V_{T0})V_{DS,A}-V_{DS,A}^2\right] \qquad I_{D,A} = \frac{k_{driver}}{2}\left[2(V_{GS,B}-V_{T0})V_{DS,B}-V_{DS,B}^2\right]$$

$$I_D = I_{D,A} = I_{D,B} = \frac{I_{D,A}+I_{D,B}}{2}$$

$$I_D = \frac{k_{driver}}{4}\left[2(V_{GS,B}-V_{T0})(V_{DS,A}+V_{DS,B})-(V_{DS,A}+V_{DS,B})^2\right]$$

$$I_D = \frac{k_{driver}}{4}\left[2(V_{GS}-V_{T0})V_{DS}-V_{DS}^2\right]$$

Two nMOS transistors connected in series and with the same gate voltage behave like *one* nMOS transistor with $k_{eq} = 0.5k_{driver}$

Generalized NAND structure with Multiple inputs

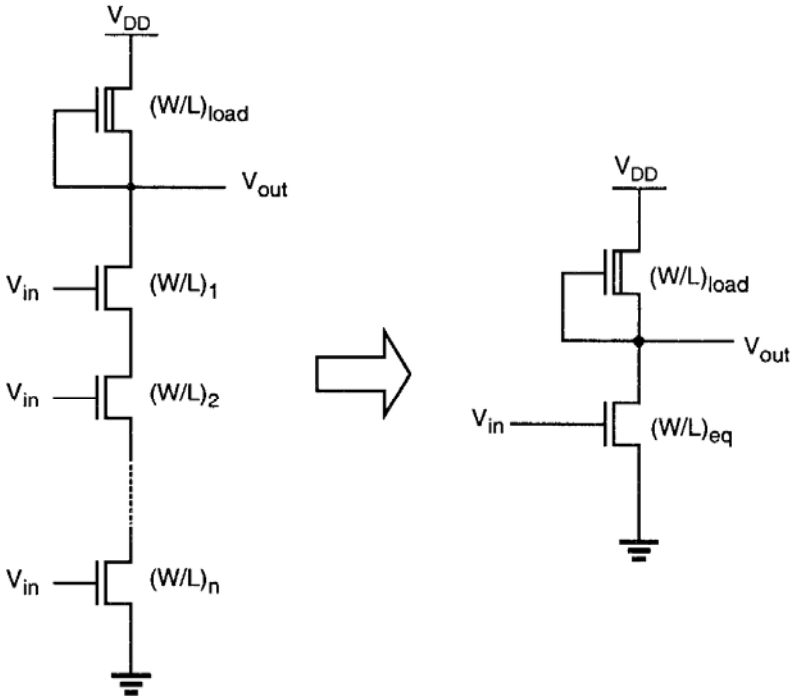


Figure 7.8 The generalized NAND structure and its inverter equivalent.

$$ID = \frac{\mu_n C_{ox}}{2}\left(\frac{1}{\sum_{k(on)}\frac{1}{\left(\frac{W}{L}\right)}}\right)\cdot\begin{cases}\left[2(V_{in}-V_{T0})V_{out}-V_{out}^2\right] & \textit{linear}\\ (V_{in}-V_{T0})^2 & \textit{saturation}\end{cases}$$

$$\left(\frac{W}{L}\right)_{equivalent} = \frac{1}{\sum_{k(on)}\frac{1}{\left(\frac{W}{L}\right)_k}}$$

$$\left(\frac{W}{L}\right)_{equivalent} = \frac{1}{n}\left(\frac{W}{L}\right)$$

Transient analysis of NAND gate

$V_A = V_{OH}$ and other input V_B is switching from V_{OH} to V_{OL}

both the output voltage V_{out} and the internal node voltage V_x will rise

$$C_{load} = C_{gd,load} + C_{gd,A} + C_{gd,B} + C_{gs,A} + C_{db,A} + C_{db,B} + C_{sb,A} + C_{sb,load} + C_{wire}$$

V_B is equal to V_{OH} and V_A switches from V_{OH} to V_{OL}

the output voltage V_{out} will rise, but the internal node voltage V_x will remain low

because the bottom driver transistor is on

$$C_{load} = C_{gd,load} + C_{gd,A} + C_{db,A} + C_{sb,load} + C_{wire}$$

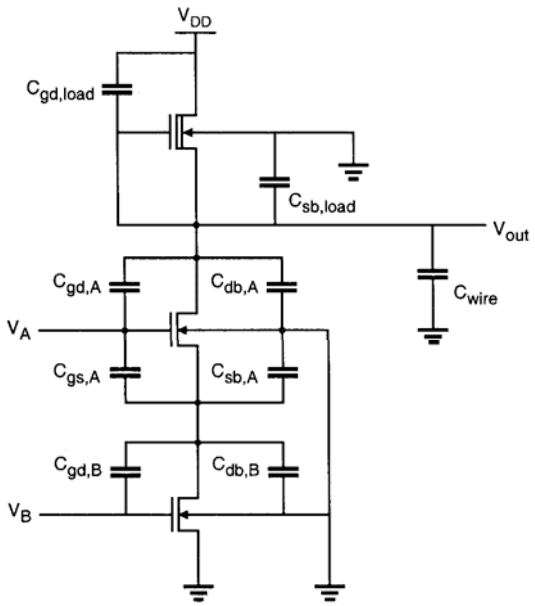
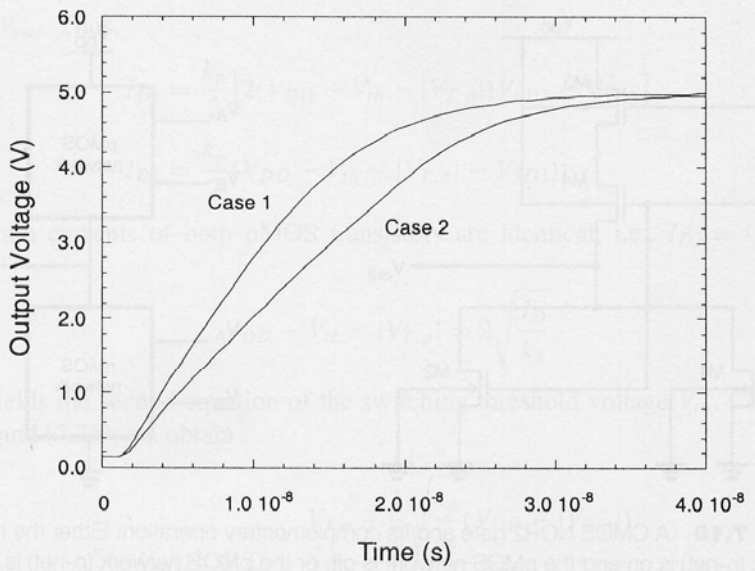


Figure 7.9 Parasitic device capacitances in the NAND2 gate.

Example 7.1

A depletion-load nMOS NAND2 gate is simulated with SPICE for two different input switching events. The SPICE input file of the circuit is listed in the following. Note that the total capacitance between the intermediate node X and the ground is assumed to be half of the total capacitance appearing between the output node and the ground.

```
NAND2 circuit delay analysis
m1 3 1 0 0 mn w=5u l=1u
m2 4 2 3 0 mn w=5u l=1u
m3 5 4 4 0 mnd w=1u l=3u
c1 4 0 0.1p
cp 3 0 0.05p
vdd 5 0 dc 5.0
* case 1 (upper input switching from high to low)
vin1 2 0 dc pulse (5.0 0.0 1ns 1ns 2ns 40ns 50ns)
vin2 1 0 dc 5.0
* case 2 (lower input switching from high to low)
* vin1 2 0 dc 5.0
* vin2 1 0 dc pulse (5.0 0.0 1ns 1ns 2ns 40ns 50ns)
.model mn nmos (vto=1.0 kp=25u gamma=0.4)
.model mnd nmos (vto=-3.0 kp=25u gamma=0.4)
.tran 0.1ns 40ns
.print tran v(1) v(2) v(4)
.end
```



The simulated transient response of the NAND2 gate for both cases is plotted against time above. The time delay difference between the two cases is clearly visible. In fact, the propagation delay time in Case 2 is about 30% larger than that in Case 1, which proves that the input switching order has a significant influence on speed.

CMOS logic circuits

- CMOS NOR2 gate
- CMOS NAND2 gate
- Layout of simple CMOS logic gates

CMOS NOR2 gate

- Consisting
  - A parallel-connected n-net
  - A series-connected complementary p-net
- Operation
  - Either one or both input are high
    - The n-net creates a conduction path between the output node
    - The p-net is cut off
    - Output low, V_{OL}=0
  - Both input are low
    - The n-net is cut off
    - The p-net creates a conduction path between the output node and V_{DD}
    - Output high, $V_{OH}=V_{DD}$

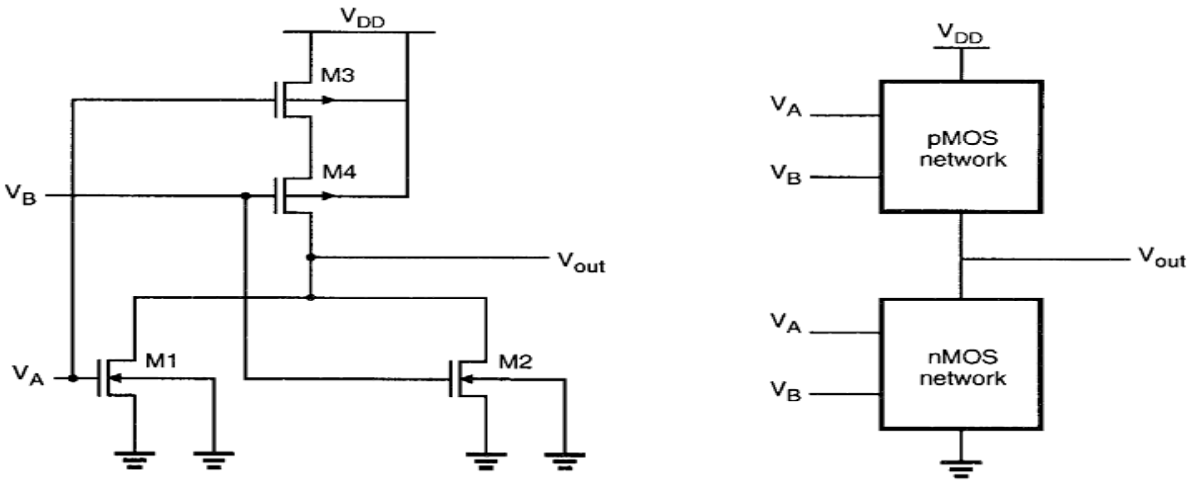


Figure 7.10 A CMOS NOR2 gate and its complementary operation: Either the nMOS network (n-net) is on and the pMOS network is off, or the pMOS network (p-net) is on and the nMOS network is off.

The switching threshold voltage

By definition, the output voltage is equal the input voltage at the switching threshold: $V_A = V_B = V_{out} = V_{th}$

Both transistors are saturated at this point, because $V_{GS} = V_{DS}$

then $I_D = k_n\left(V_{th} - V_{T,n}\right)^2 \Rightarrow V_{th} = V_{T,n} + \sqrt{\frac{I_D}{k_n}}$ (7.32)

At $V_{in} = V_{out}$, M3 in linear region, M4 in saturation region

$I_{D3} = \frac{k_p}{2}\left[2\left(V_{DD} - V_{th} - \left|V_{T,p}\right|\right)V_{SD3} - V_{SD3}^2\right]$, $I_{D4} = \frac{k_p}{2}\left(V_{DD} - V_{th} - \left|V_{T,p}\right| - V_{SD3}\right)^2$

$I_{D3} = I_{D4} \Rightarrow V_{DD} - V_{th} - \left|V_{T,p}\right| = 2\sqrt{\frac{I_D}{k_p}}$ (7.35), Conbining (7.32) and (7.35)

$V_{th}\left(NOR2\right) = \frac{V_{T,n} + \frac{1}{2}\sqrt{\frac{k_p}{k_n}}\left(V_{DD} - \left|V_{T,p}\right|\right)}{1 + \frac{1}{2}\sqrt{\frac{k_p}{k_n}}}$ (7.36), $V_{th}\left(INR\right) = \frac{V_{T,n} + \sqrt{\frac{k_p}{k_n}}\left(V_{DD} - \left|V_{T,p}\right|\right)}{1 + \sqrt{\frac{k_p}{k_n}}}$ (CMOS inverter)

If $k_n = k_p$ *and* $V_{T,n} = \left|V_{T,p}\right|$, $V_{th(CMOS\ inverter)} = V_{DD}/2$, $V_{th}\left(NOR2\right) = \frac{V_{DD} + V_{T,n}}{3}$, not equal to $V_{DD}/2$

For example: $VDd = 5V, V_{T,n} = \left|V_{T,p}\right| = 1V, V_{th}(NOR2) = 2V, V_{th}(INR) = 2.5V$

The switching threshold voltage

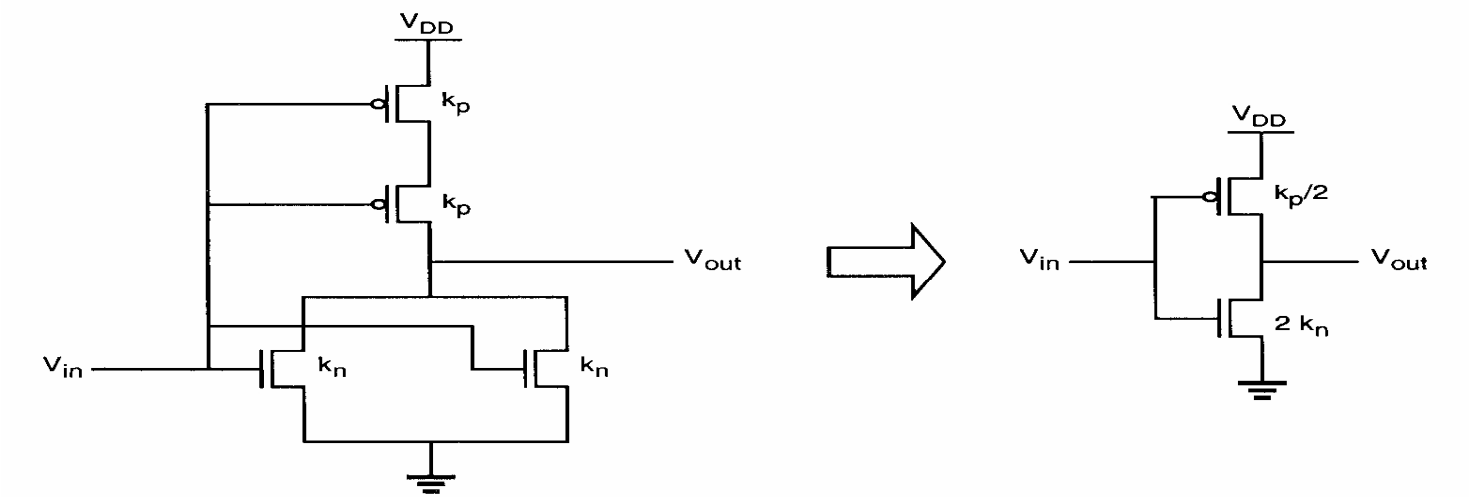


Figure 7.11 A CMOS NOR2 gate and its inverter equivalent.

- Wh
  - The parallel-connected nMOS transistors can be represented by a single nMOS transistor with $2k_n$
  - The series-connected pMOS transistors are represented by a single pMOS transistor with $k_p/2$
  - Using the inverter switching threshold expression (7.37) for the equivalent inverter circuit
    - $$V_{th}(NOR2) = \frac{V_{T,n} + \sqrt{\frac{k_p}{4k_n}}\left(V_{DD} - |V_{T,p}|\right)}{1 + \sqrt{\frac{k_p}{4k_n}}}$$
    - In order to achieve Vth=VDD/2, we have to set $V_{T,n}=|V_{T,p}|$ and $k_p=4k_n$

CMOS NAND2 gate

- The n-net in series, the p-net in parallel.

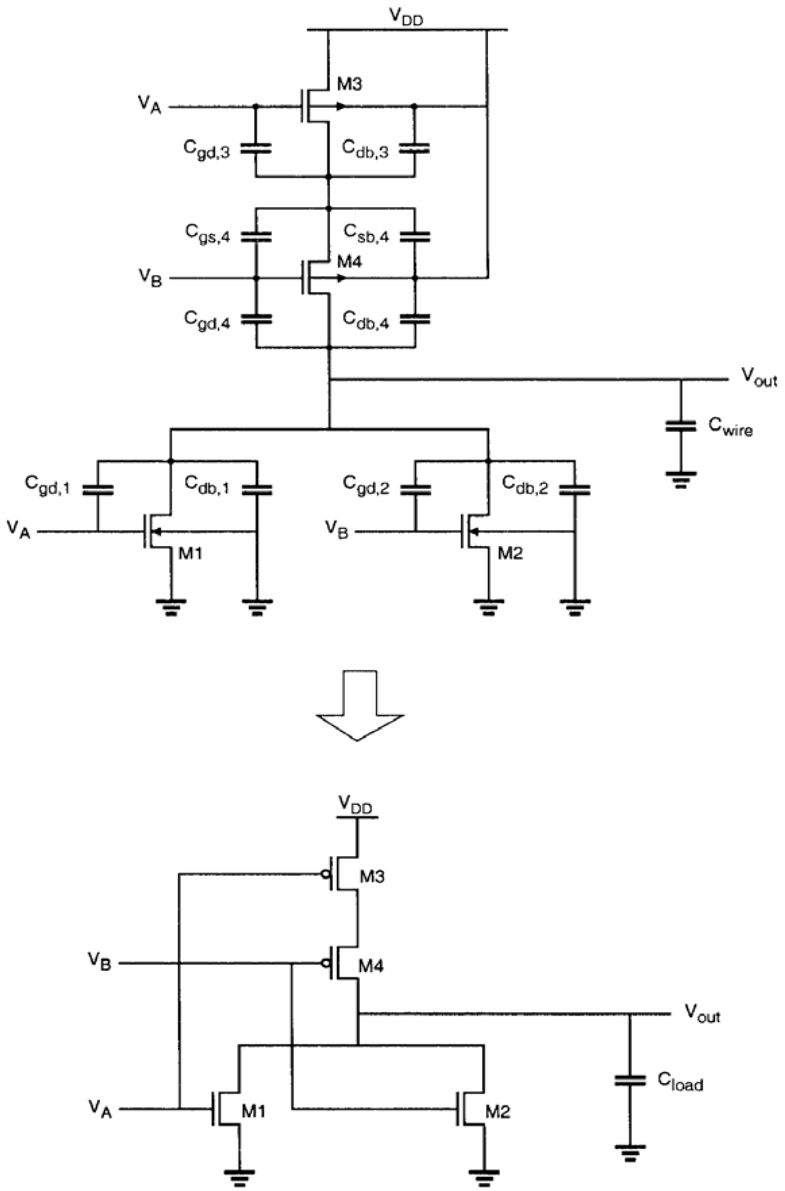


Figure 7.12 Parasitic device capacitances of the CMOS NOR2 circuit and the simplified equivalent with the lumped output load capacitance.

NAND2's inverter equivalent

- Assuming $(W/L)_{n,A}=(W/L)_{n,B}$ and $(W/L)_{p,A}=(W/L)_{p,B}$
  - The switching threshold
    - $$V_{th}(NAND2)=\frac{V_{T,n}+\sqrt{\frac{k_p}{k_n}}\left(V_{DD}-\left|V_{T,p}\right|\right)}{1+2\sqrt{\frac{k_p}{k_n}}}$$
    - A threshold voltage of $V_{DD}/2$ is achieved by setting $V_{T,n}=|V_{T,p}|$ and $k_n=4k_p$

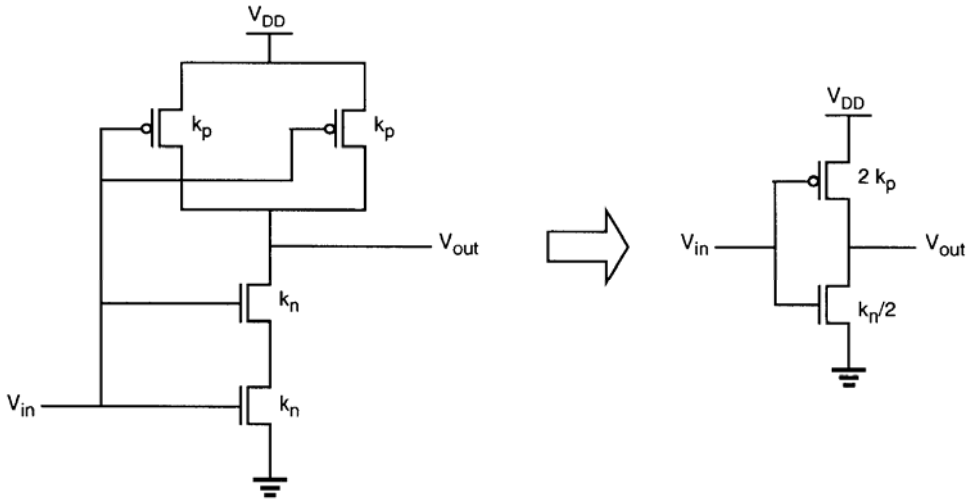


Figure 7.13 A CMOS NAND2 gate and its inverter equivalent.

Layout of simple CMOS logic gates

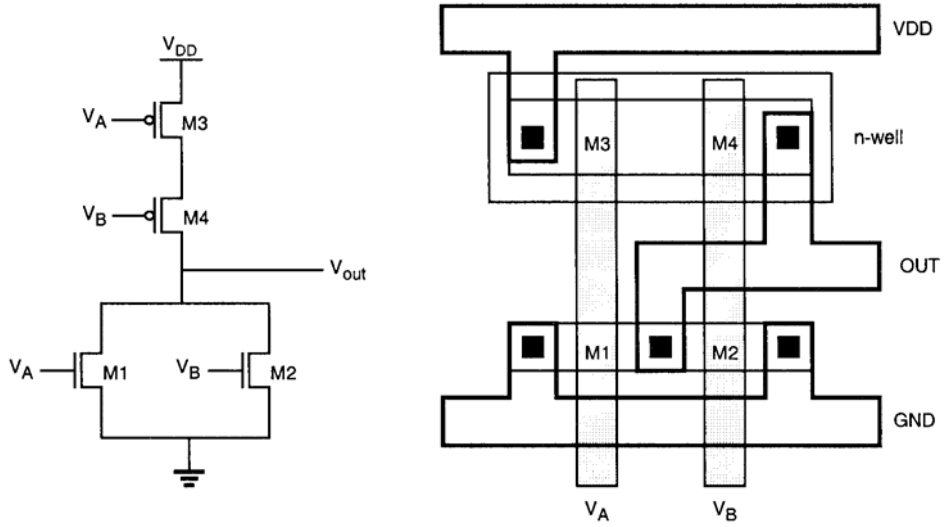


Figure 7.14 Sample layout of the CMOS NOR2 gate.

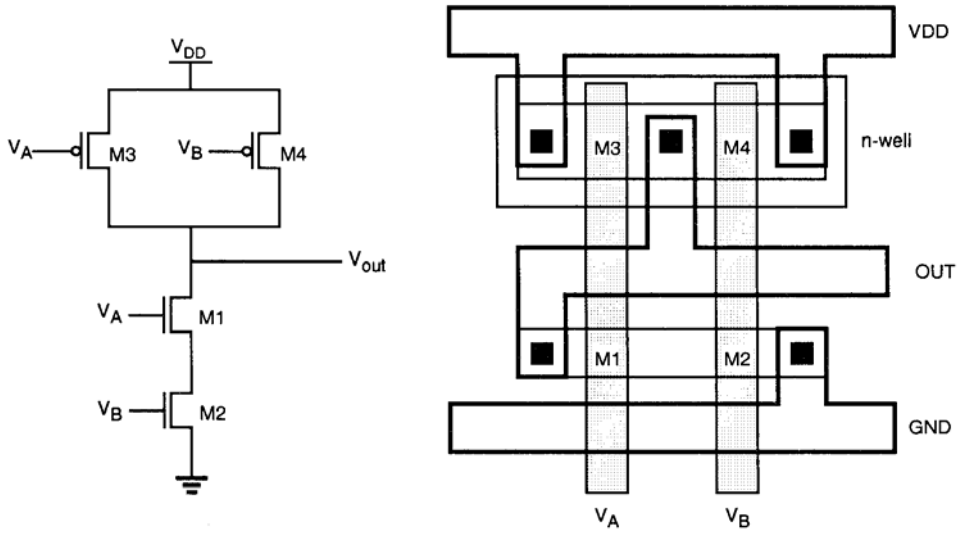


Figure 7.15 Sample layout of the CMOS NAND2 gate.

Stick-diagram layout of the CMOS NOR2 gate

- The stick-diagram does not carry out any information on the actual geometry relations of the individual features, but it conveys valuable information on the relative placement of the transistors and their interconnections

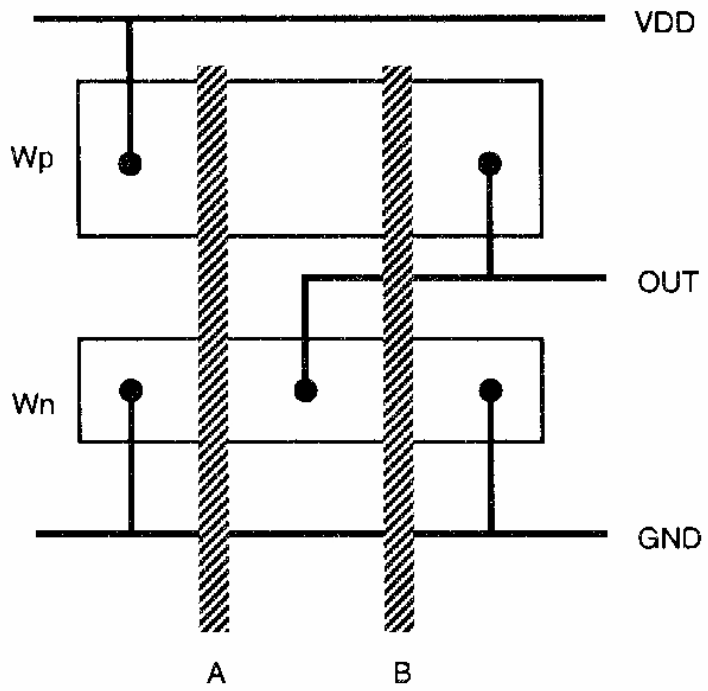


Figure 7.16 Stick-diagram layout of the CMOS NOR2 gate.

Complex logic circuits

- The simple design principle of the pull-down network
  - OR operations are performed by parallel-connected drivers
  - AND operations are performed by series-connected drivers
  - Inversion is provided by the nature of MOS circuit operation
- If all input variables are logic high, the equivalent-driver (W/L) ratio of the pull-down network
  - $Z = \overline{A(D+E)+BC}$

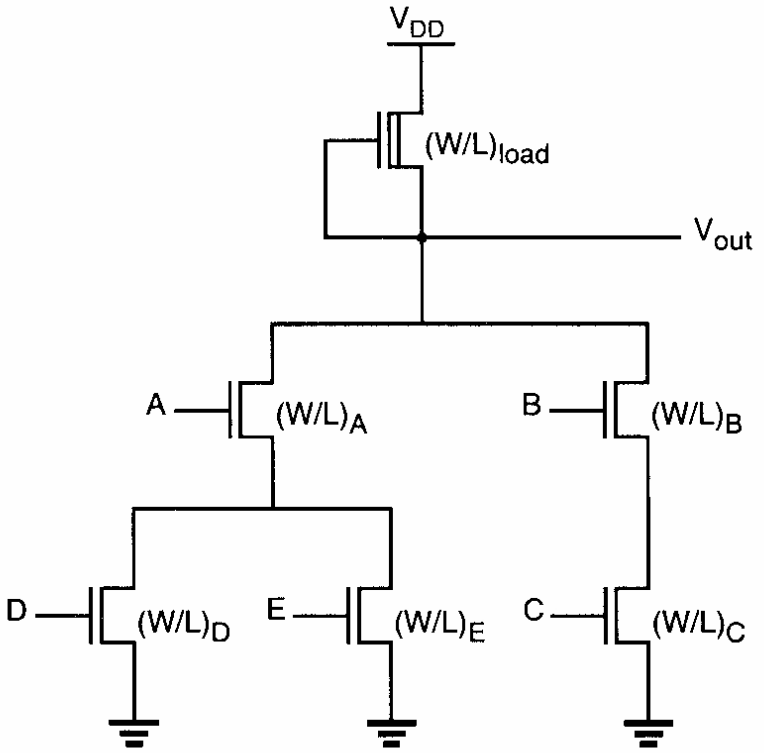


Figure 7.17 nMOS complex logic gate realizing the Boolean function given in (7.41).

$$\left(\frac{W}{L}\right)_{equivalent} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_B}+\frac{1}{\left(\frac{W}{L}\right)_C}} + \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_A}+\frac{1}{\left(\frac{W}{L}\right)_D+\left(\frac{W}{L}\right)_E}}$$

Complex logic circuits

- For calculating the logic-low voltage level V_{OL}
  - The value of VOL depends on the number *and* the configuration of the conducting nMOS transistors
  - Assigning a class number which reflects the total resistance of the current path from V_{out} node to ground
    - A-D $\Rightarrow$ class 1 $\Rightarrow$ highest series resistance
    - A-E $\Rightarrow$ class 1$\Rightarrow$ highest series resistance
    - B-C $\Rightarrow$ class 1$\Rightarrow$ highest series resistance
    - A-D-E $\Rightarrow$ class 2
    - A-D-B-C $\Rightarrow$ class 3
    - A-E-B-C $\Rightarrow$ class 3
    - A-D-E-B-C $\Rightarrow$ class 4
- $V_{OL1}>V_{OL2}>V_{OL3}>V_{OL4}$
- We usually start by specifying a maximum V_{OL} value

- The design objective$\Rightarrow$ determine the driver and load transistor size$\rightarrow$ achieves the specified V_{OL} value even in the worst case
- Three worst-case paths
  - $$\left(\frac{W}{L}\right)_A = \left(\frac{W}{L}\right)_D = 2\left(\frac{W}{L}\right)_{driver}$$
    $$\left(\frac{W}{L}\right)_A = \left(\frac{W}{L}\right)_E = 2\left(\frac{W}{L}\right)_{driver}$$
    $$\left(\frac{W}{L}\right)_B = \left(\frac{W}{L}\right)_C = 2\left(\frac{W}{L}\right)_{driver}$$
  - Guarantee all other input $\Rightarrow$ output low will less than V_{OL}

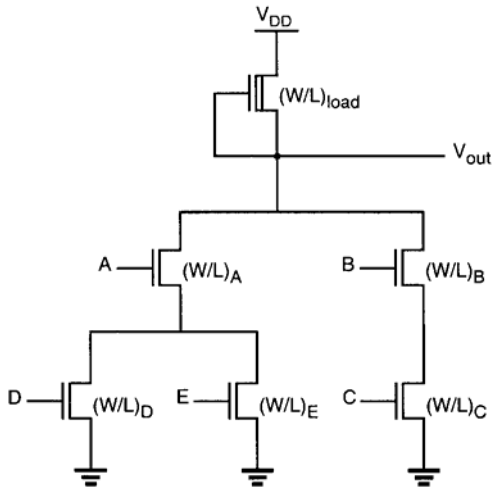


Figure 7.17 nMOS complex logic gate realizing the Boolean function given in (7.41).

Complex CMOS logic gates

- The pMOS pull-up network
  - Must be the dual network of the n-net
    - nMOS parallel ⇒ pMOS series
    - nMOS series ⇒ pMOS parallel

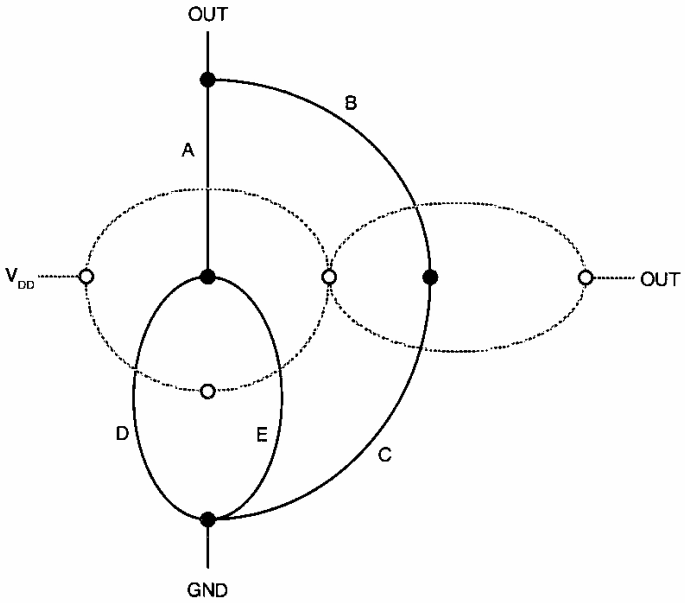


Figure 7.18 Construction of the dual pull-up graph from the pull-down graph, using the dual-graph concept.

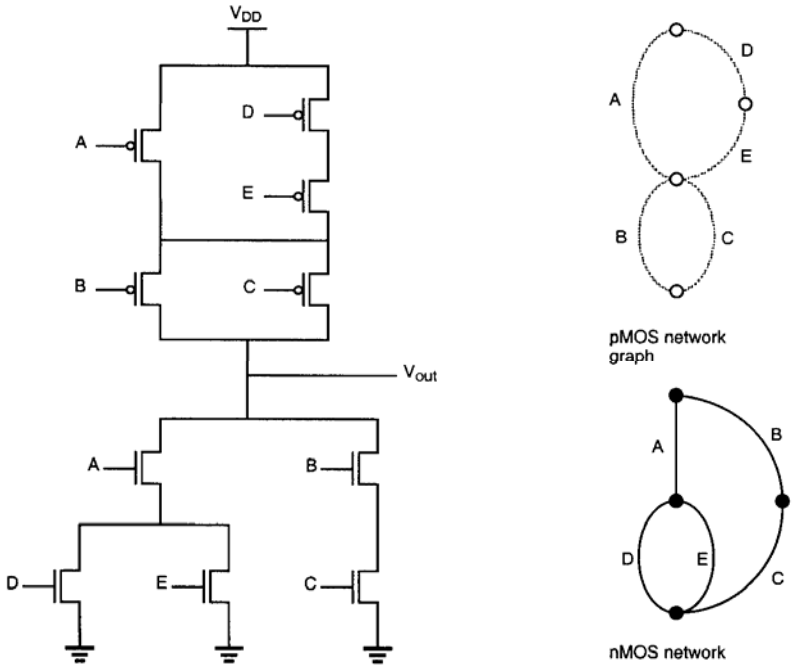


Figure 7.19 A complex CMOS logic gate realizing the Boolean function (7.41).

Stick-diagram, with arbitrary ordering of poly-Si

- The stick diagram layout ⇒ a “first attempt”
- An arbitrary ordering of the polysilicon gate column
  - The separation between polysilicon must be allow
    - One diffusion-to-diffusion separation
    - Two metal-to-diffusion contacts
  - Consuming area

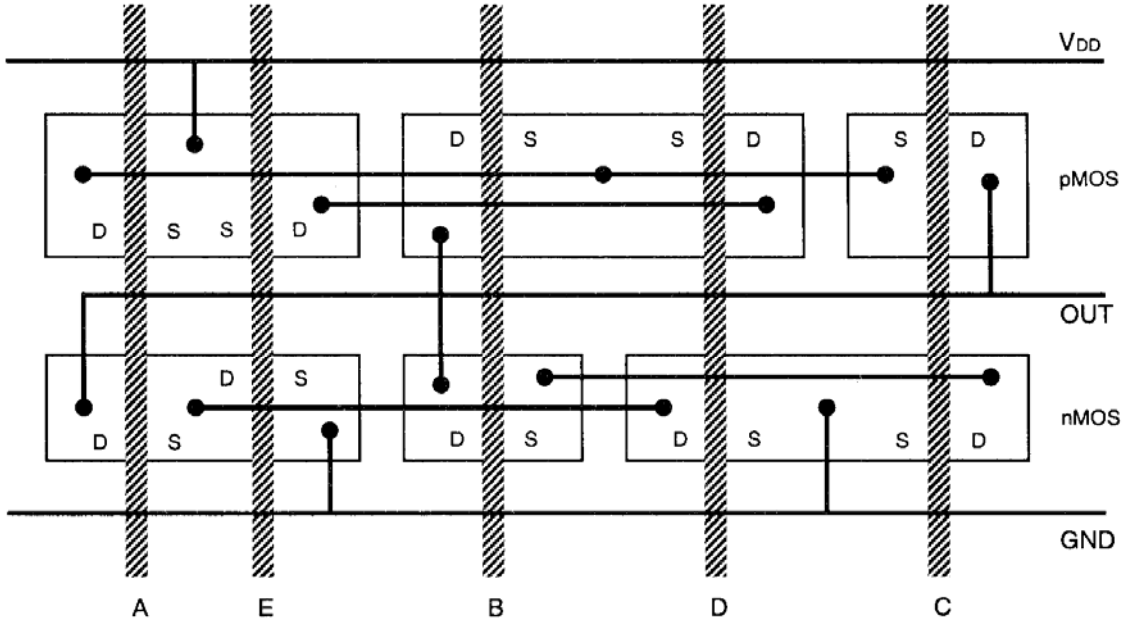


Figure 7.20 Stick-diagram layout of the complex CMOS logic gate, with an arbitrary ordering of the polysilicon gate columns.

Stick-diagram, Euler path approach

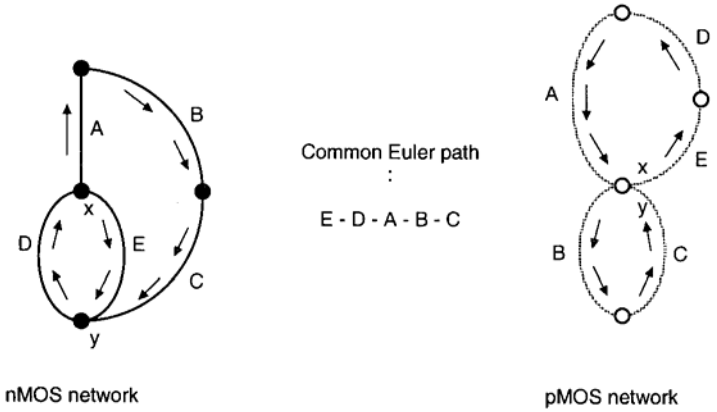


Figure 7.21 Finding a common Euler path in both graphs for n-net and p-net provides a gate ordering that minimizes the number of diffusion breaks and, thus, minimizes the logic-gate layout area. In both cases, the Euler path starts at (x) and ends at (y).

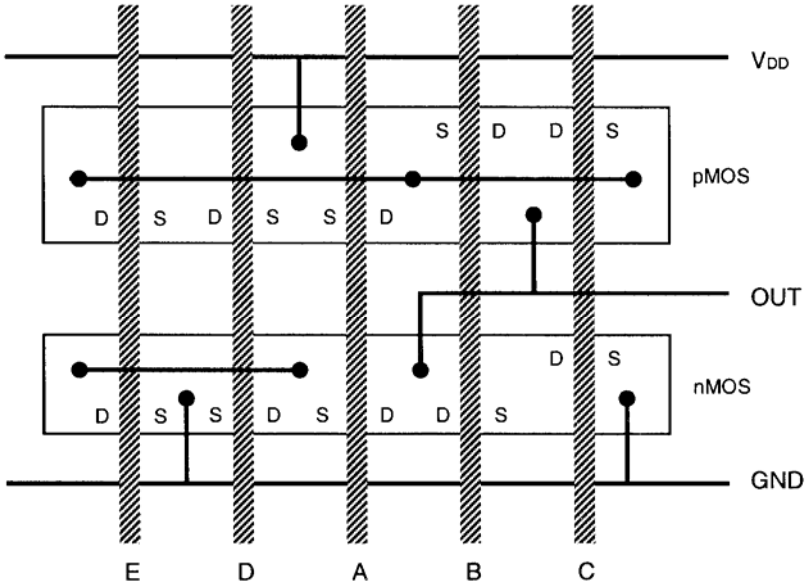


Figure 7.22 Optimized stick-diagram layout of the complex CMOS logic gate.

- Find a Euler-path in the pull-down graph and a Euler path in the pull-up graph with identical ordering of input labels
- The Euler path is defined as an uninterrupted path that traverses each edge (branch) of the graph exactly once
  - E-D-A-B-C
- The polysilicon column separation has to allow
  - Only metal-to-diffusion contact
- More compact layout area, simple routing of signals, less parasitic capacitance

Full CMOS implementation of XOR

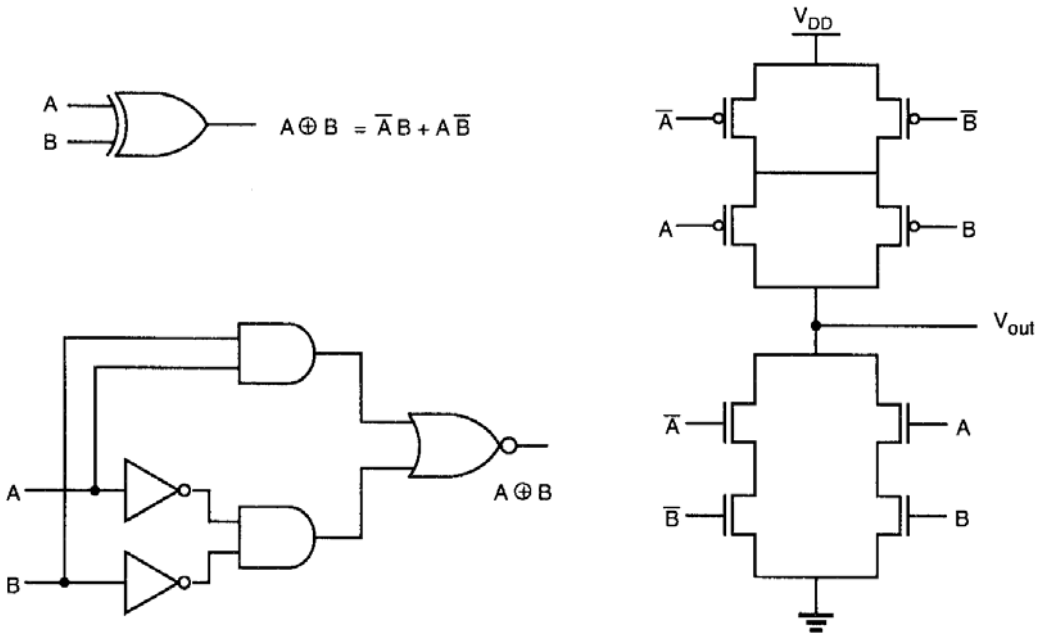


Figure 7.23 Full-CMOS implementation of the XOR function.

- Two additional inverter are needed
- Total 12 transistors

AOI and OAI gates

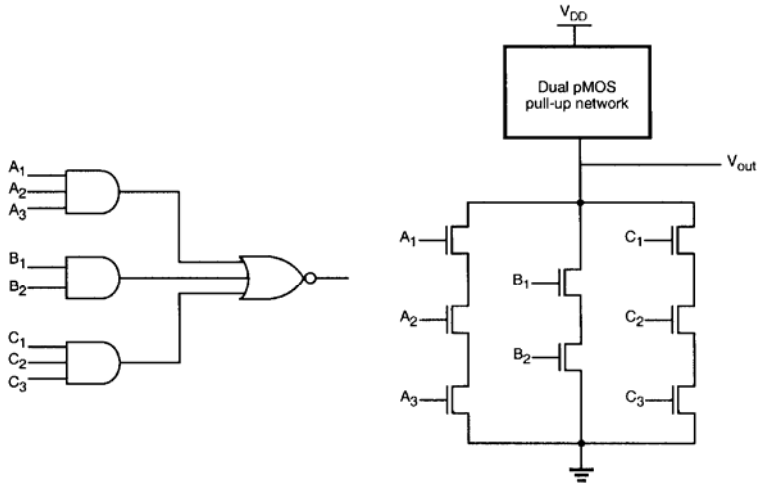


Figure 7.24 An AND-OR-INVERT (AOI) gate and the corresponding pull-down net.

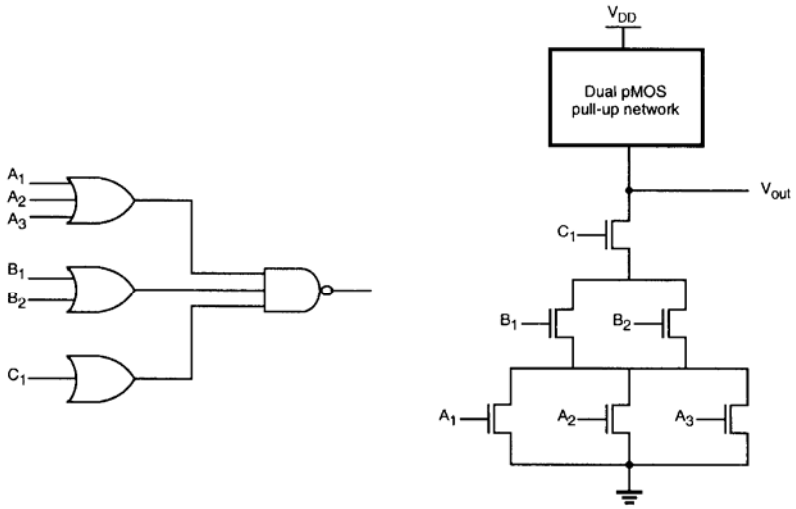


Figure 7.25 An OR-AND-INVERT (OAI) gate, and the corresponding pull-down net.

- The AOI gates
  - Enable the sum-of-products realization of a Boolean function in one logic stage
- The OAI gates
  - Enable the product-of-sums realization of a Boolean function in one logic stage

Psuedo-nMOS gates

- CMOS gates $\Rightarrow$ large area
- Pseudo-nMOS
  - To reduce the number of transistors
  - To use a single pMOS transistor as the load device
    - with its gate terminal connected to ground
  - Disadvantage
    - Nonzero static power dissipation
      - As the V_{out} is lower than $V_{DD} \Rightarrow$ the always-on pMOS load device conducts a steady state current
    - The value of V_{OL} and the noise margins
      - Determining by the ratio of pMOS transconductance load to driver transconductance

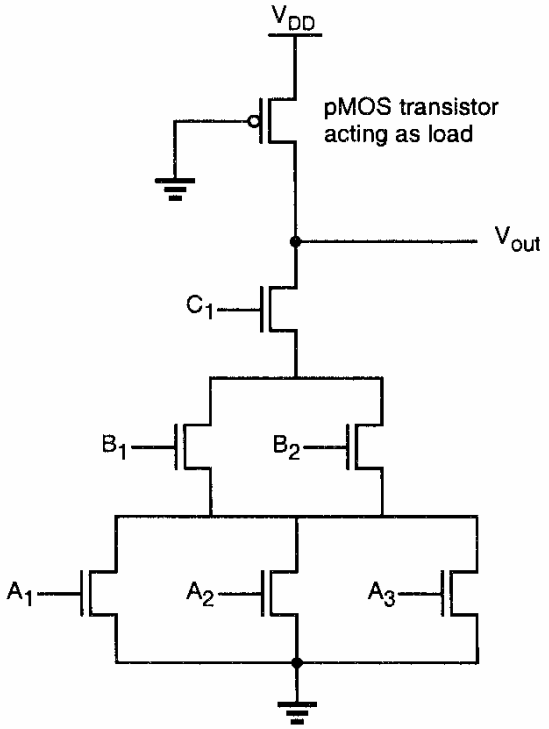
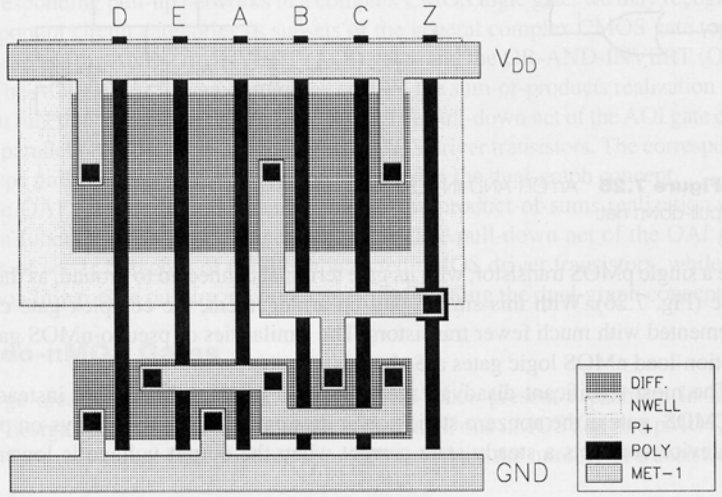


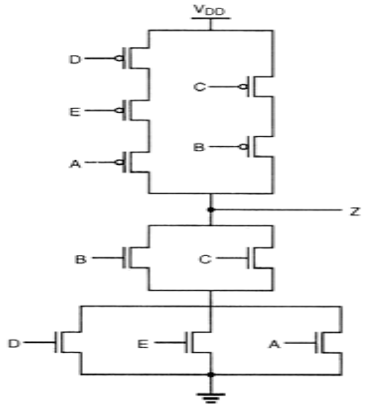
Figure 7.26 The pseudo-nMOS implementation of the OAI gate in Fig. 7.25.

Example 7.2

The simplified layout of a CMOS complex logic circuit is given below. Draw the corresponding circuit diagram, and find an equivalent CMOS inverter circuit for simultaneous switching of all inputs, assuming that $(W/L)_p = 15$ for all pMOS transistors and $(W/L)_n = 10$ for all nMOS transistors.



The circuit diagram can be found from the layout by inspection:



The Boolean function realized by this circuit is

$$Z = \overline{(D + E + A)(B + C)}$$

The equivalent (W/L) ratios of the nMOS network and the pMOS network are determined by using the series-parallel equivalency rules discussed earlier in this chapter, as follows.

$$\left(\frac{W}{L}\right)_{n,eq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_D + \left(\frac{W}{L}\right)_E + \left(\frac{W}{L}\right)_A} + \frac{1}{\left(\frac{W}{L}\right)_B + \left(\frac{W}{L}\right)_C}}$$

$$= \frac{1}{\frac{1}{30} + \frac{1}{20}} = 12$$

$$\left(\frac{W}{L}\right)_{p,eq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_D} + \frac{1}{\left(\frac{W}{L}\right)_E} + \frac{1}{\left(\frac{W}{L}\right)_A}} + \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_B} + \frac{1}{\left(\frac{W}{L}\right)_C}}$$

$$= \frac{1}{\frac{1}{15} + \frac{1}{15} + \frac{1}{15}} + \frac{1}{\frac{1}{15} + \frac{1}{15}} = 12.5$$

CMOS full-adder circuit_gate level

- The carry_out signal to generate the sum output
  - Reduce the circuit complexity
  - Save chip area

$$sum\_out = A \oplus B \oplus C$$

$$= ABC + A\overline{B}\,\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{C}B$$

$$carry\_out = AB + AC + BC$$

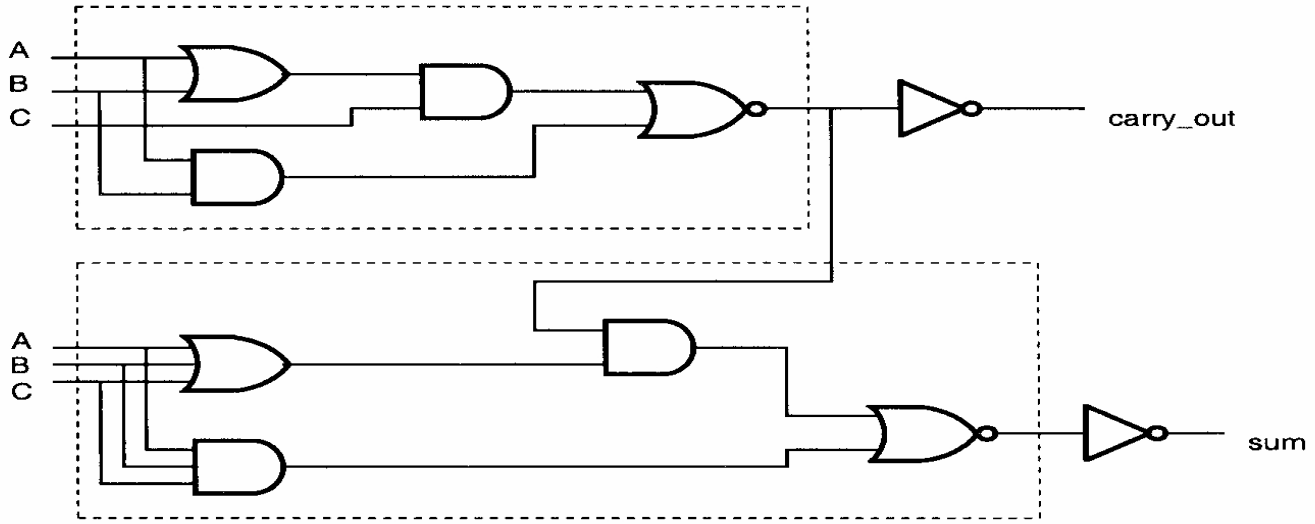


Figure 7.27 Gate-level schematic of the one-bit full-adder circuit.

CMOS full-adder circuit

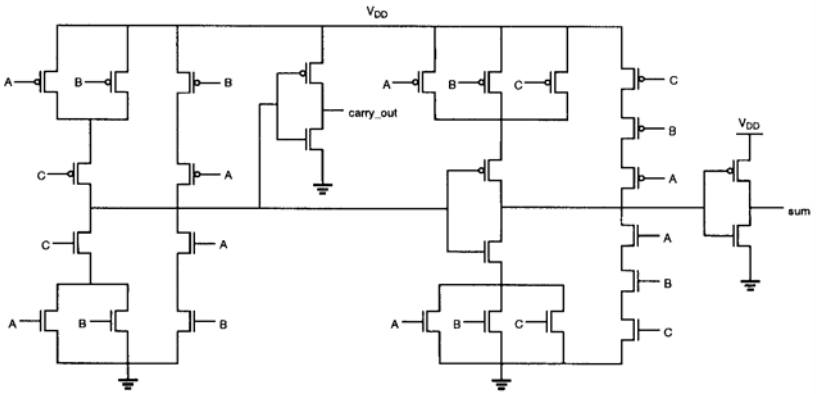


Figure 7.28 Transistor-level schematic of the one-bit full-adder circuit.

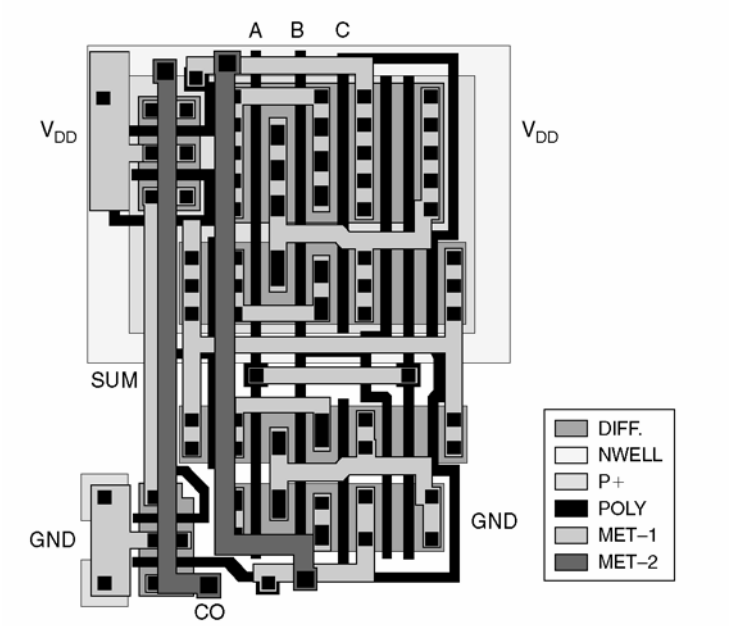


Figure 7.30 Mask layout of the optimized CMOS full adder circuit.

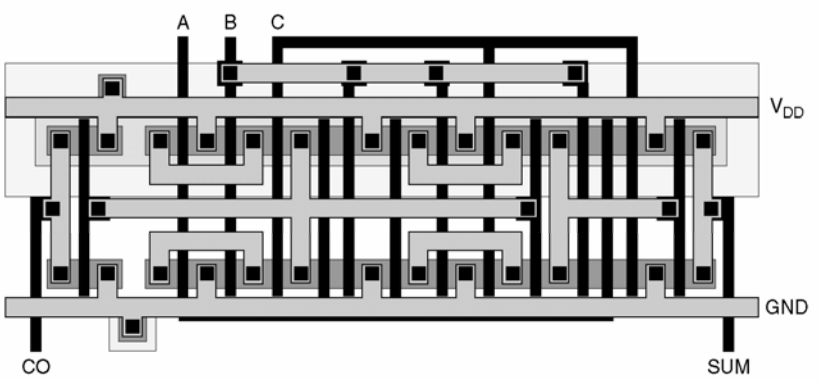


Figure 7.29 Mask layout of the CMOS full-adder circuit using minimum-size transistors.

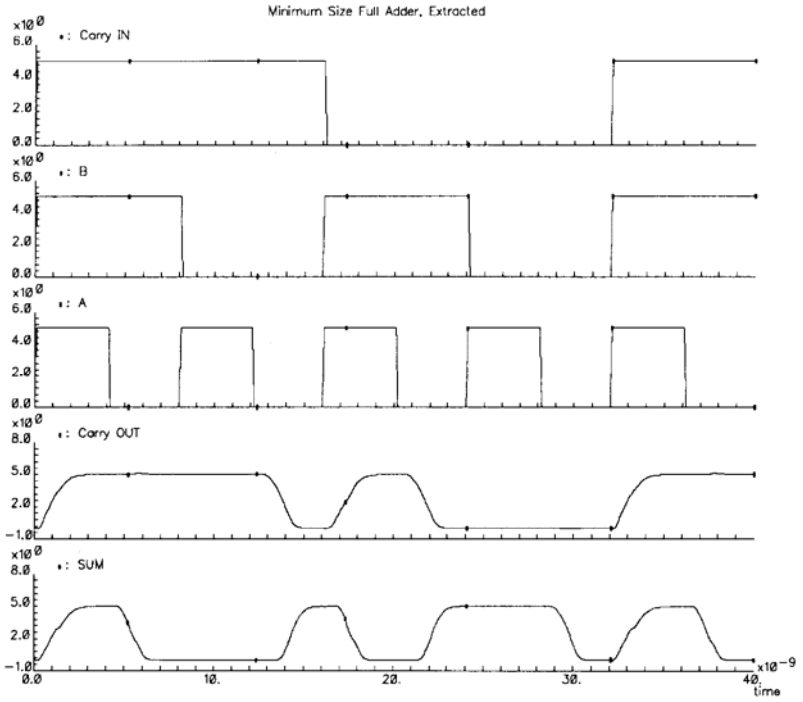


Figure 7.31 Simulated input and output waveforms of the CMOS full-adder circuit.

CMOS transmission gates (pass gates)

- Consisting of one nMOS and one pMOS transistor, connected in parallel
- The gate voltage applied to these two transistors are also set to be complementary signals
- A bidirectional switch between nodes A and B which is controlled by signal C
  - If signal C is logic high
    - Low-resistance current path between the nodes A and B
  - If the signal C is low
    - Both transistors will be off
- Both transistors must take into account the substrate-bias effect

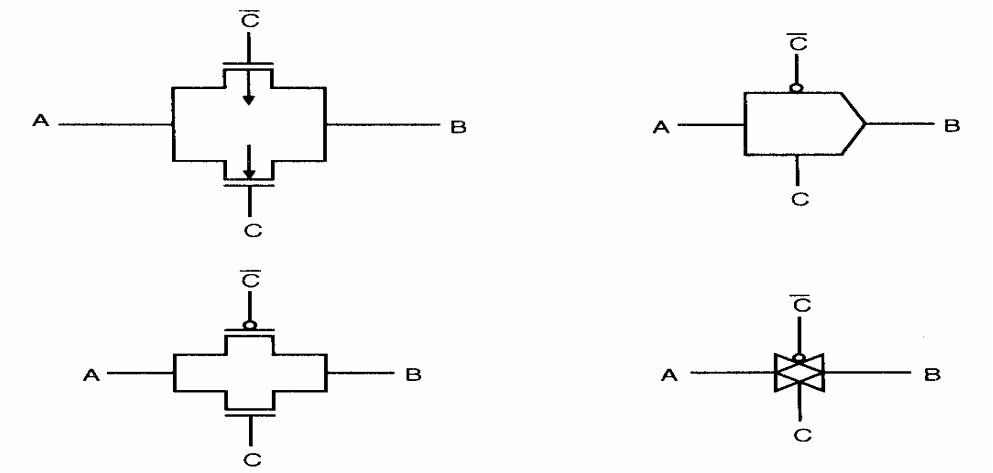


Figure 7.33 Four different representations of the CMOS transmission gate (TG).

Carry ripple adder

- N-bit binary adder
  - The full adder as the basic building block
  - Two n-bit binary numbers as input and produces the binary sum at the output
  - The overall speed of the carry ripple adder is obviously limited by
    - The delay of the carry bits rippling through the carry chain
    - A fast carry_out response become essential
    - Critical path

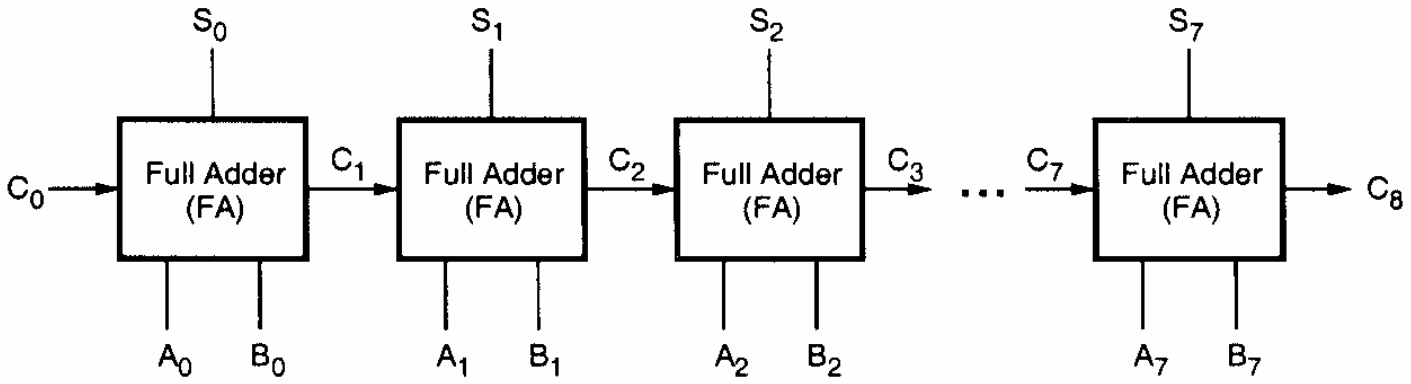


Figure 7.32 Block diagram of a carry ripple adder chain consisting of full adders.

CMOS transmission gates (pass gates)

- Consisting of one nMOS and one pMOS transistor, connected in parallel
- The gate voltage
  - Complementary signal to the two transistors
- Bidirectional switch between A and B, controlled by C
  - Signal C is logic-high
    - Both transistors turn on, low resistance current path
  - Signal C is logic-low
    - Both transistors turn off, open, high-impedance state
  - Substrate terminal
    - nMOS⇒ ground, pMOS ⇒ VDD
    - Must consider body effect

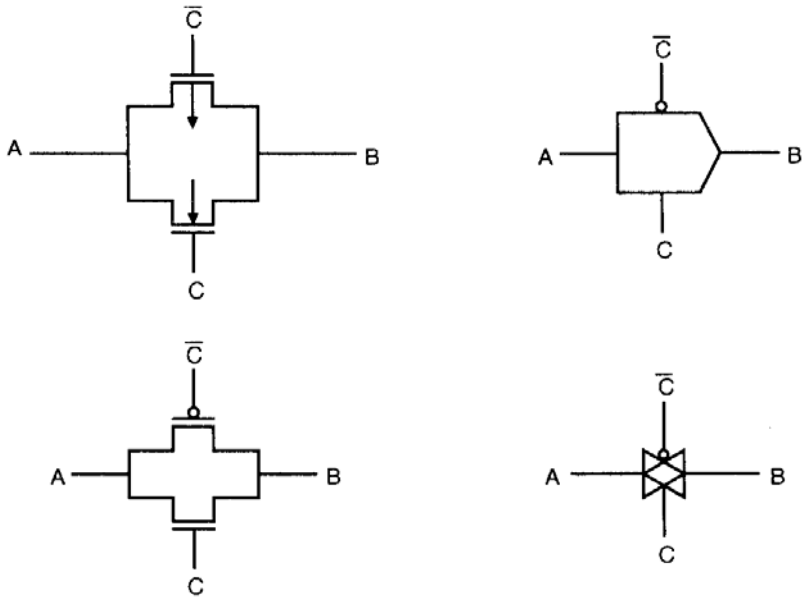


Figure 7.33 Four different representations of the CMOS transmission gate (TG).

CMOS transmission gates (pass gates)

$V_{in} = V_{DD}$, The control signal is logic - high, the output node may be connected to a capacitor

For *nMOS* transistor $\Rightarrow V_{DS,n} = V_{DD}\text{-}V_{out}$, $V_{GSn} = V_{DD}\text{-}V_{out}$

The *nMOS* will turn off for $V_{out} > V_{DD}\text{-}V_{T,n}$ and operate in the saturation for $V_{out} < V_{DD}\text{-}V_{T,n}$

For *pMOS* transistor $\Rightarrow V_{DS,p} = V_{out}\text{-}V_{DD}$, $V_{GS,p} = \text{-}V_{DD}$

The *pMOS* is in saturation for $V_{out} < |V_{T,p}|$, in linear region for $V_{out} > |V_{T,p}|$, *pMOS* remains turn on, regardless of the V_{out}

The total current : $I_D = I_{DS,n} + I_{SD,p}$

equivalent resistance : $R_{eq,n} = \dfrac{V_{DD}\text{-}V_{out}}{I_{DS,n}}$, $R_{eq,p} = \dfrac{V_{DD}\text{-}V_{out}}{I_{SD,p}}$, The total resistance = $R_{eq,n} \| R_{eq,p}$

Region 1

$V_{out} < |V_{T,p}| \Rightarrow$ both transistor in saturation, $R_{eq,n} = \dfrac{2(V_{DD}\text{-}V_{out})}{k_n(V_{DD} - V_{out} - V_{T,n})^2}$, $R_{eq,p} = \dfrac{2(V_{DD}\text{-}V_{out})}{k_p(V_{DD} - |V_{T,p}|)^2}$

note that $V_{SB,n} = V_{out}$, $V_{SB,p} = 0 \Rightarrow$ *nMOS* should take into account the sbustrate - bias effect

Region 2

$|V_{T,p}| < V_{out} < (V_{DD} - V_{T,n}) \Rightarrow$ *pMOS* linear region, *nMOS* saturation region

$$R_{eq,n} = \frac{2(V_{DD}\text{-}V_{out})}{k_n(V_{DD} - V_{out} - V_{T,n})^2},\ R_{eq,p} = \frac{2(V_{DD}\text{-}V_{out})}{k_p\left[2(V_{DD} - |V_{T,p}|)(V_{DD}\text{-}V_{out}) - (V_{DD} - |V_{T,p}|)^2\right]} = \frac{2}{k_p\left[2(V_{DD} - |V_{T,p}|) - (V_{DD} - V_{out})\right]}$$

Region 3

$V_{out} > (V_{DD} - V_{T,n}) \Rightarrow$ *pMOS* linear region, *nMOS* off

$$R_{eq,p} = \frac{2}{k_p\left[2(V_{DD} - |V_{T,p}|) - (V_{DD} - V_{out})\right]}$$

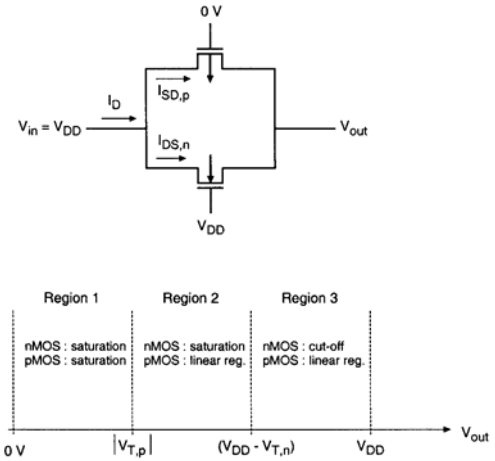


Figure 7.34 Bias conditions and operating regions of the CMOS transmission gate, shown as functions of the output voltage.

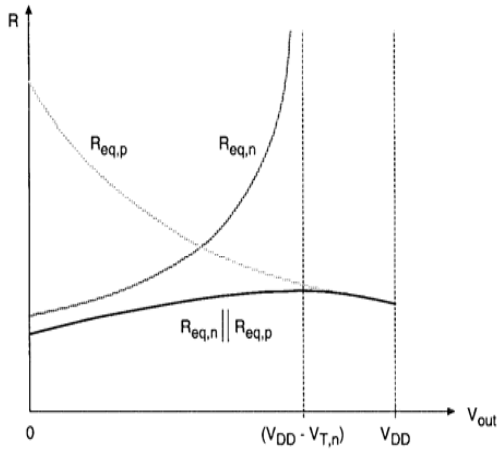


Figure 7.35 Equivalent resistance of the CMOS transmission gate, plotted as a function of the output voltage.

Replacing the CMOS TG with its resistor equivalent

- The total equivalent resistance of the TG remains relatively constant
  - Its value is almost independent of the output voltage
    - Whereas the individual equivalent resistances are strongly dependent on V_{out}
  - A CMOS TG can be replaced by its simple equivalent resistance for dynamic analysis

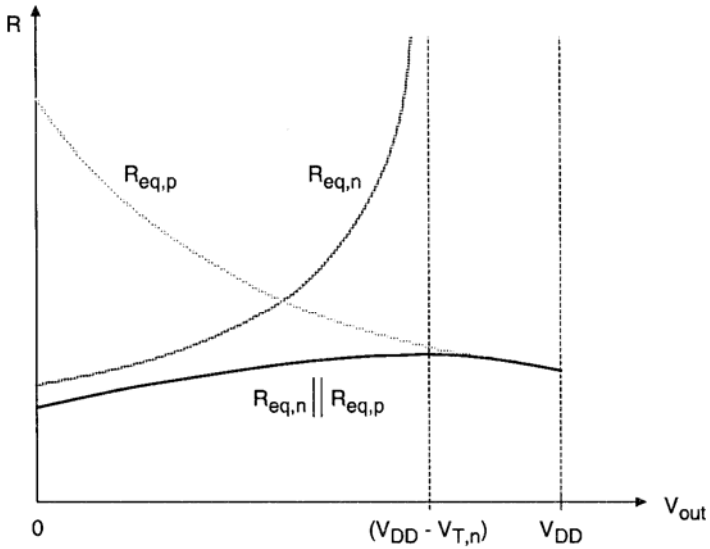


Figure 7.35 Equivalent resistance of the CMOS transmission gate, plotted as a function of the output voltage.

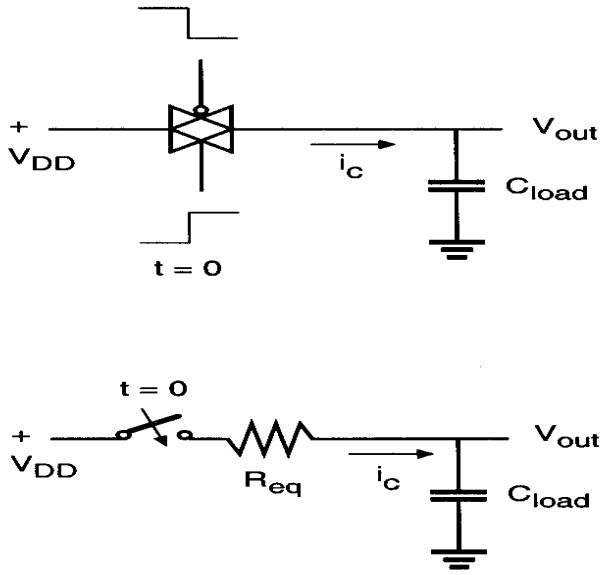


Figure 7.36 Replacing the CMOS TG with its resistor equivalent for transient analysis.

Two input multiplexer

- The implement of CMOS transmission gates in logic circuit design
  - Compact circuit structures, requires a smaller number of transistors
  - The control signal and its complement must be available simultaneously for TG applications
- Two input multiplexer
  - If the control input S is logic high
    - The bottom TG conduct $\Rightarrow$ output equal to the input B
  - If the control input S is logic low
    - The top TG conduct $\Rightarrow$ output equal to the input A

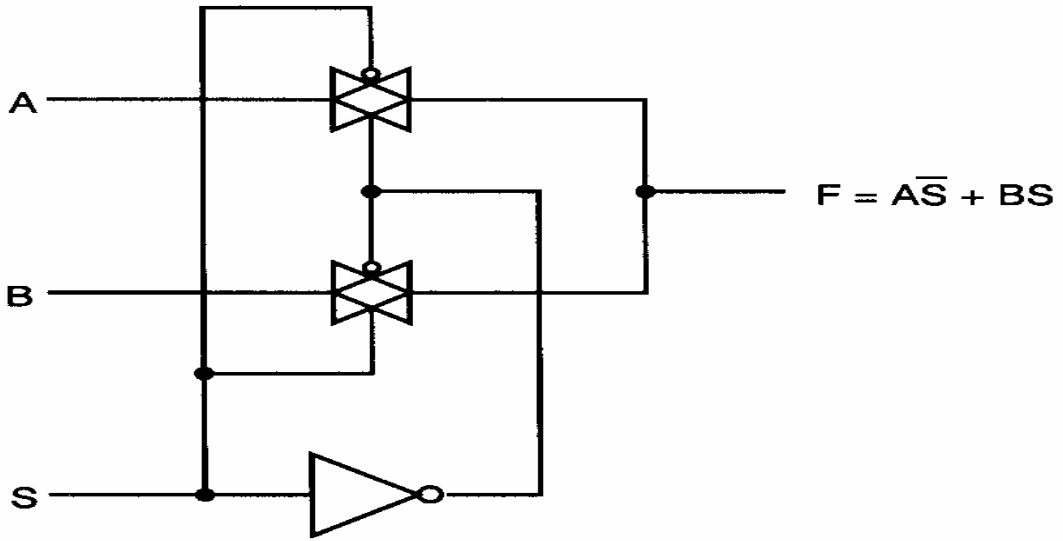


Figure 7.37 Two-input multiplexer circuit implemented using two CMOS TGs.

XOR

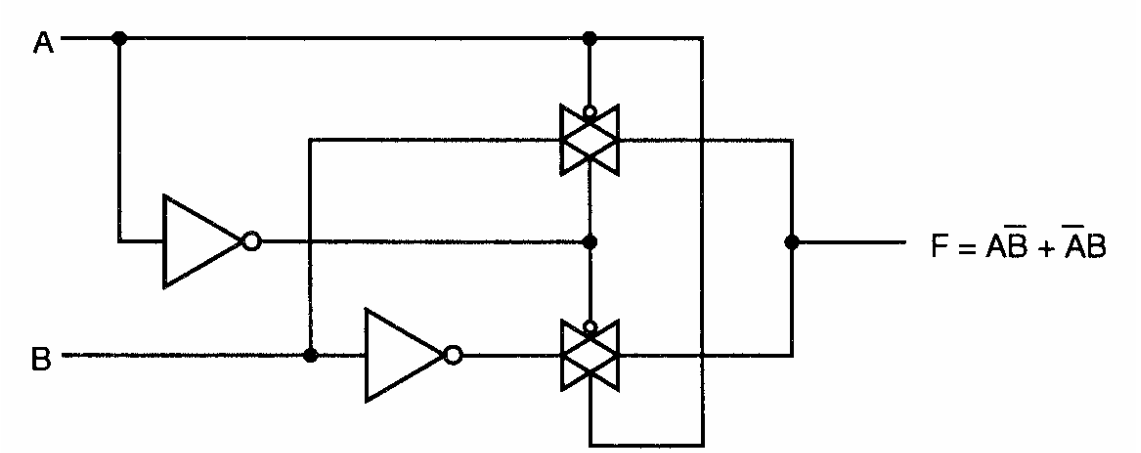


Figure 7.38 Eight-transistor CMOS TG implementation of the XOR function.

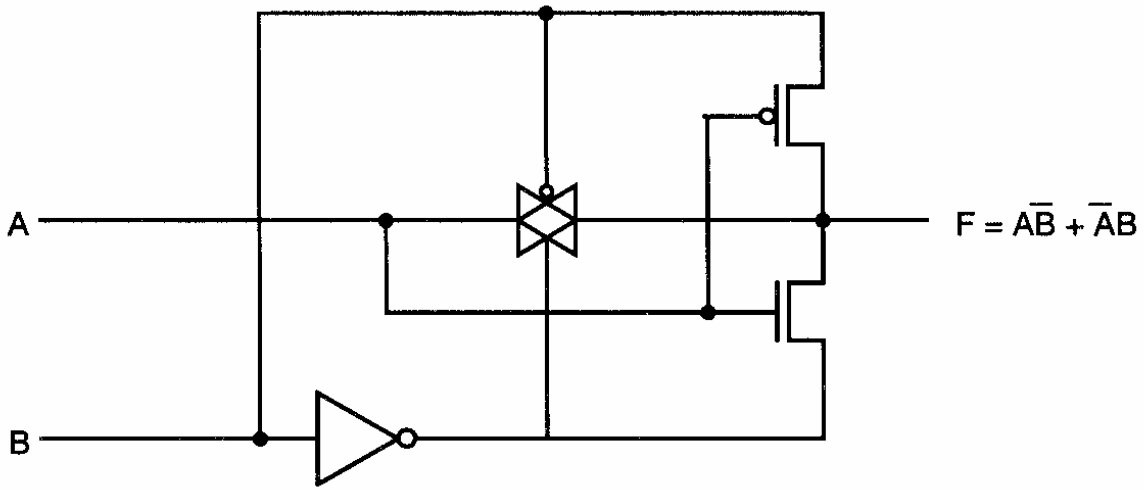


Figure 7.39 Six-transistor CMOS TG implementation of the XOR function.

CMOS TG realization of a three-variable Boolean function

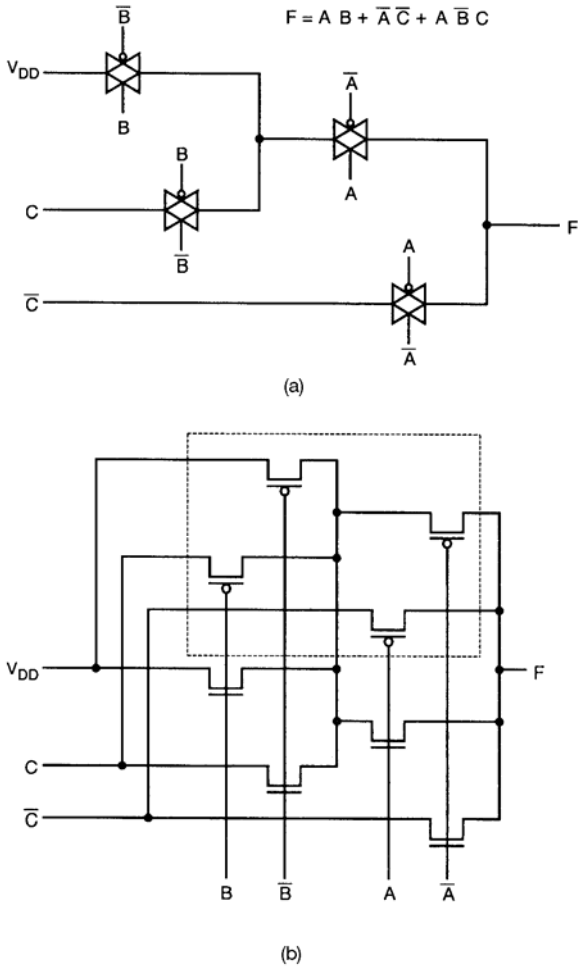


Figure 7.40 (a) CMOS TG realization of a three-variable Boolean function. (b) All pMOS transistors can be placed into one n-well to save area.

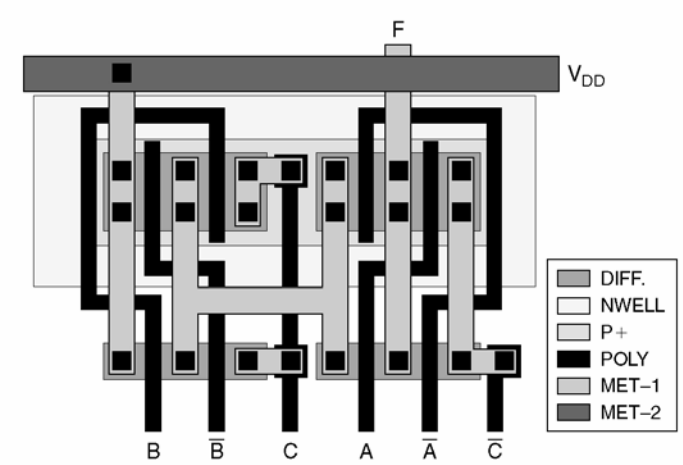


Figure 7.41 Mask layout of the CMOS TG circuit shown in Fig. 7.40.

Complementary pass-transistor logic (CPL)

- The main idea behind CPL is to use a purely nMOS pass-transistor network for the logic operations, instead of a CMOS TG network
  - All input are applied in complementary form
  - The circuit also produces complementary outputs, to be used by subsequent CPL stage
  - The CPL circuit consisting
    - Complementary input
    - An nMOS pass transistor logic network to generate complementary outputs
    - CMOS output inverter to restore the output signal

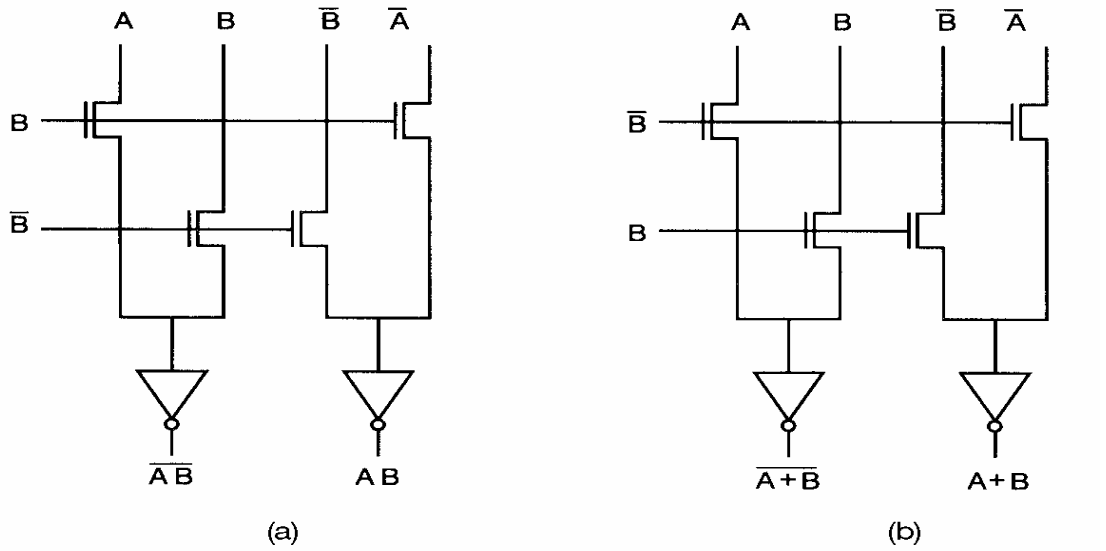


Figure 7.42 Circuit diagram of (a) CPL NAND2 gate and (b) CPL NOR2 gate.

Complementary pass-transistor logic

- The elimination of pMOS transistors from the pass-gate network
  - Reducing the parasitic capacitances
  - Higher operation speed
  - Process complexity
    - The $V_{t,n}$ must be reduced to about 0V through threshold-adjustment implants
      - Reducing the overall noise immunity
      - Making the transistors more susceptible to subthreshold conduction in the off-mode
  - The CPL design style is highly modular
    - A wide range of functions can be realized by using the same basic pass-transistor structures

Regarding the transistor count

- CPL circuits do not always offer a marked advantage over conventional CMOS
- NAND2, NOR2⇒8 transistors
- XOR, XNOR functions realized with CPL have a similar complexity as CMOS realizations
  - The cross-coupled pMOS pull-up transistors are used to speed up the output response
- Full adder
  - The same observation is true for the realization with CPL
  - consisting of 32 transistors

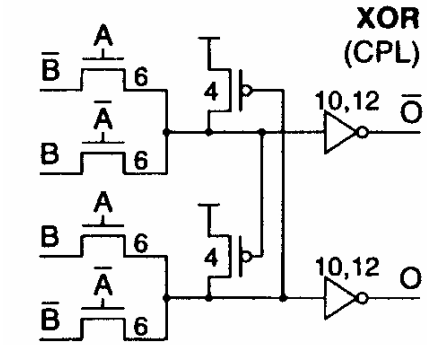


Figure 7.43 Circuit diagram of a CPL-based XOR gate.

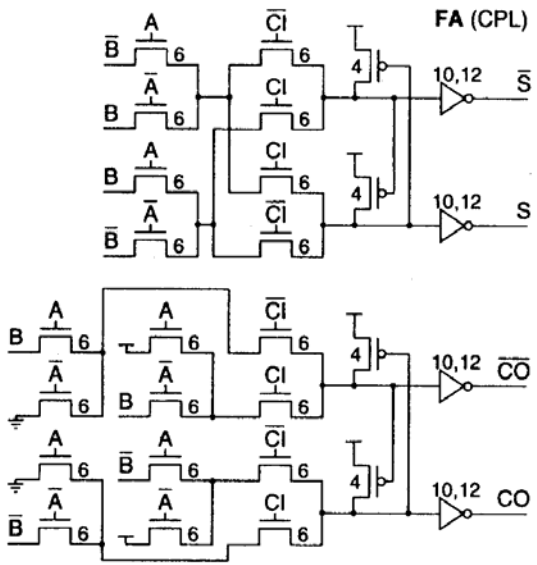


Figure 7.44 Circuit diagram of a CPL full adder.

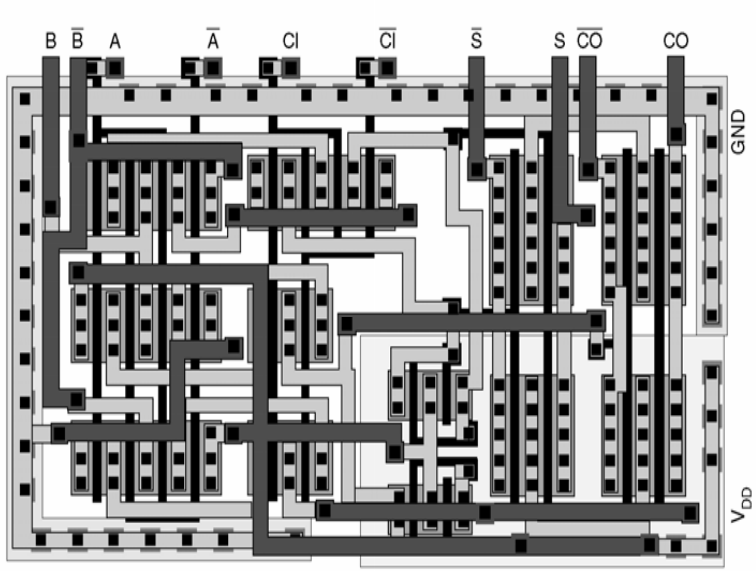


Figure 7.45 Mask layout of the CPL full adder shown in Fig. 7.44.