ASSIGNMENT 02
VLSI DESIGN

Question 1. Draw the design hierarchy of 4 bit sequence detector.

Question 2. Using Matlab, verify the I_{ds}-V_{ds} curve of Mosfet in Linear region.

Question 3. Write a short note on

a) LOCOS(local oxide of silicon)
b) CMOS fabrication Step with required figure.
c) Write down the sign of the following parameter with reference to PMOS and NMOS
   1. Fermi-Potential φ_F
   2. Depletion region Charge Density Q_{B0} and Q_B
   3. Substrate bias coefficient γ
   4. Substrate bias Voltage
d) Prove that the threshold voltage for the Mosfet including other effect is given by

$$V_T = V_{T0} + \gamma(\sqrt{|(-2\varphi_F) + V_{SB}|} + \sqrt{|(-2\varphi_F)|}$$

$$Where\ \gamma = \frac{\sqrt{2qN_A\epsilon_{si}}}{Cox}$$

e) Narrow channel effect

Question 4. i. Write a short note on oxide related capacitance and how this capacitance varies with MOSFET different Mode of operation (Cut off, linear, Saturation).

ii. Also describe the junction related capacitance with required derivation.

Question 5. Derive equation for the VOH, VOL, VIH, and VIL for depletion load NMOS inverter.

Question 6. Write a short note on

a) Sub-threshold conduction with required equation
b) Variation of mobility with electric field
c) Variation of channel length in saturation mode
d) Saturation of carrier velocity

Question 7. What do you mean by The Level 1 Model Equation for the Mosfet? Using spice determine the I_{DS}-V_{DS} curve of the Mosfet (P & N).

Question 8. An enhancement type NMOS transistor has the following parameter

V_{to}=0.8V γ=0.2$V^{0.5}$ λ=0.05V^{-1} $2\varphi_F$=0.58V K=20$\mu A/V^2$

a) When the transistor is biased with V_G=2.8V, V_D=5V, V_S=1V, and V_B=0, the drain current is I_D=0.24mA. Determine the W/L.
b) Calculate I_D for V_G=5V, V_D=4V, V_S=2V and V_B=0
c) If μ_n=500cm^2/V.s and Cg=10^{-15} F, find W/L.

Question 9. Derive the current equation for the PMOS operating in linear region for $V_{SG}+V_{TP}>V_{SD}$.