**Roll No. ……………………………………………………………**

**NEELKANTH INSTITUTE OF TECHNOLOGY**

**B.Tech ECE (Semester III)**

**FIRST SESSIONAL EXAMINATION 2015-2016**

**SWITCHING THEORY & LOGIC DESIGN (NEC-304)**

***Time: 1:30 Hours Total Marks 30***

***NOTE: - i.*** *be precise in your Answer*

***ii.*** *All section are compulsory*

**SECTION A**

1. **Attempt all the Questions: 1X10=10**
2. Determine the octal & hexadecimal equivalent of (82.25)10.

**Statement: -** In *The 7’s complement of a certain octal number is 5264. Write the answer of question b & c.*

1. Find the octal number.
2. Find Binary and hexadecimal equivalent.

***Statement: -*** *Give the next three numbers in each of the hex sequences given in question d & e*:

1. 4A5, 4A6, 4A7, 4A8, \_ \_ \_
2. B998, B999, \_ \_ \_
3. Eight-bit 2’s complement representation of (−23)10 is \_\_\_\_\_\_\_\_\_\_.
4. Given the sequence of three-bit Gray code as (000, 001, 011, 010, 110, 111, 101, 100), write the next three numbers in the four-bit Gray-code sequence after 0101.
5. Write down the Truth table of two input XOR gate.
6. What is the largest binary number that can be expressed with 16 bits? What are the equivalent decimal and hexadecimal numbers?
7. Express the boolean function F = A + B’C as sum of minterms.

**SECTION B**

1. **Attempt any Five Question : 2X5=10**
2. The solutions to the quadratic equation *x* 2 - 11x + 22 = 0 are *x* = 3 and *x* = 6. What is the base of the numbers?
3. In Hamming code write down the condition for single error correction and double error detection.
4. Implement the following POS expression using NOR-NOR logic.
5. Draw a logic diagram using only two input NOR gates to implement the following function.

F (A, B, C, D) = (A XOR B) + (C XOR D)

1. Implement the following expression using NAND-NAND logic.
2. By means of timing diagram show the signal of the output f and g in the given figure (1) as a function of two inputs a & b. Use all four possible combination a and b.



b

a

**SECTION C**

1. **Attempt any Two Questions: 5X2=10**

1. Implement the full Adder using NAND gates.
2. Find the complement of F= wx+yz then show that FF’=0 and F+F’=1. Write a short note on hamming encoder and decoder.
3. Using the tabular method obtain minimal realization of a function shown below.